DAVICOM Semiconductor, Inc.

DM9102H

Single Chip Fast Ethernet

NIC Controller

DATA SHEET

Final

Version: DM9102H-DS-F01
February 15, 2008

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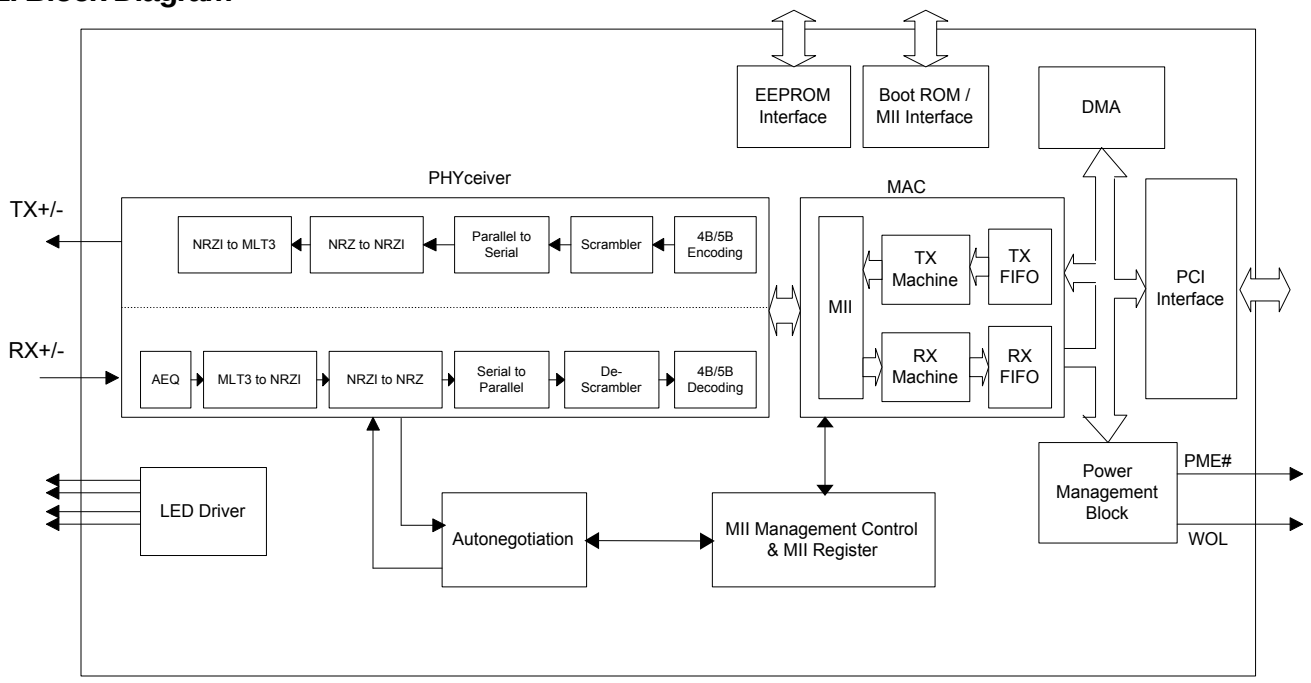
1. General Description

The DM9102H is a fully integrated and cost effective single chip Fast Ethernet NIC controller. It is designed with low power and high performance process. It is a 1.8V/3.3V device with 5V tolerance.

The DM9102H provides direct interface to the PCI bus and supports bus master mode to achieve the high performance of the PCI bus. It fully complies with PCI 2.2. In the media side, the DM9102H interfaces to the UTP3, 4, 5 in 10Base-T and the UTP5 in 100Base-TX. It is fully compliant with the IEEE 802.3u Spec. Its auto-negotiation function will automatically configure the DM9102H to take the maximum advantage of its abilities. The DM9102H also supports IEEE 802.3x's full-duplex flow control.

The DM9102H supports two types of power management mechanisms. The main mechanism is based on the On Now architecture, which is required for PC99. The alternative mechanism is based upon the remote Wake-On-LAN mechanism.

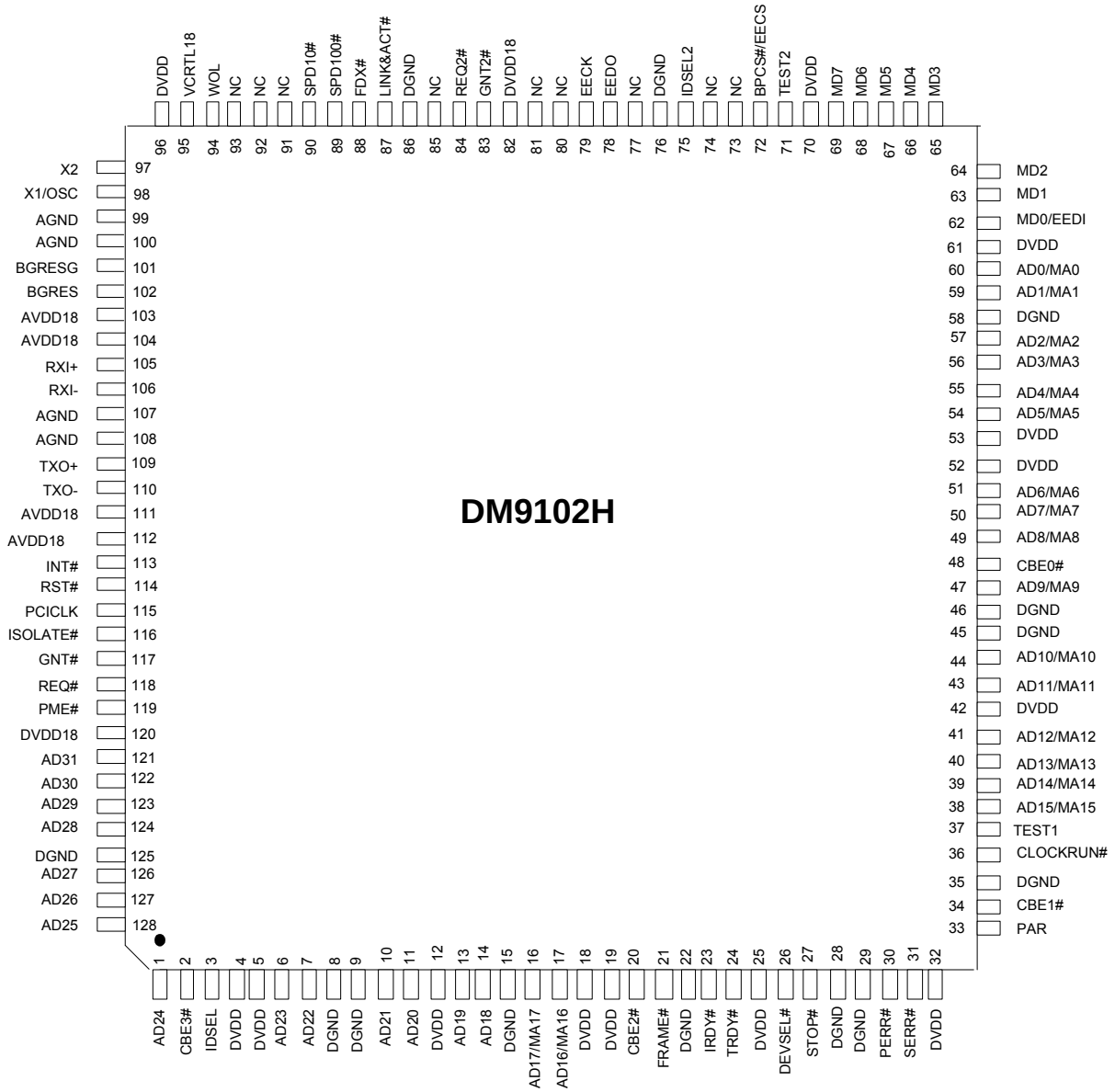
2. Block Diagram



3. Features

- Integrated Fast Ethernet MAC, Physical Layer and Transceiver in one chip.
- Comply with PCI specification 2.2.
- PCI clock up to 66MHz.
- PCI bus master architecture.
- PCI bus burst mode data transfer.
- Two large independent transmission and receipt of FIFO
- Support transmit threshold under-run re-try mode
- Up to 256K bytes Boot EPROM or Flash interface.
- EEPROM 93C46 interface automatically supports node ID load and configuration information.
- Comply with IEEE 802.3u 100Base-TX and 802.3 10Base-T.
- Comply with IEEE 802.3u auto-negotiation protocol for automatic link type selection.
- Support IEEE 802.3x Full Duplex Flow Control
- VLAN frame length support.
- IP/TCP/UDP checksum generation and checking
- Comply with ACPI and PCI Bus Power Management.
- Support the MII (Media Independent Interface) for an external PHY
- Support Wake-On-LAN function and remote wake-up (Magic packet, Link Change and Microsoft® wake-up frame).
- Support 4 Wake-On-LAN (WOL) signals (active high pulse, active low pulse, and active high, active low.)
- High performance 100Mbps clock generator and data recovery circuit.
- Digital clock recovery circuit, using advanced digital algorithm to reduce jitter.
- Provides Loopback mode for easy system diagnostics.
- Support auto-MDIX
- +1.8/3.3V Power supply with +5V tolerant I/O.
- 128 pin LQFP with CMOS process.

4. Pin Configuration: 128 pin LQFP



5. Pin Description

I = Input, O = Output, I/O = Input / Output, O/D = Open Drain, P = Power,
LI = reset Latch Input, # = asserted Low

5.1 PCI Bus Interface Signals

Pin No. 128LQFP	Pin Name	I/O	Description
113	INT#	O/D	Interrupt Request This signal will be asserted low when an interrupted condition as defined in CR5 is set, and the corresponding mask bit in CR7 is cleared.
114	RST#	I	System Reset When this signal is low, the DM9102H performs the internal system reset to its initial state.
115	PCICLK	I	PCI system clock PCI bus clock that provides timing for DM9102H related to PCI bus transactions. The clock frequency range is up to 40MHz.
117	GNT#	I	Bus Grant This signal is asserted low to indicate that DM9102H has been granted ownership of the bus by the central arbiter.
118	REQ#	O	Bus Request The DM9102H will assert this signal low to request the ownership of the bus.
119	PME#	O/D	Power Management Event. Open drain. Active Low. The DM9102H drives it low to indicate that a power management event has occurred.
3	IDSEL	I	Initialization Device Select This signal is asserted high during the Configuration Space read/write access.
21	FRAME#	I/O	Cycle Frame This signal is driven low by the DM9102H master mode to indicate the beginning and duration of a bus transaction.
23	IRDY#	I/O	Initiator Ready This signal is driven low when the master is ready to complete the current data phase of the transaction. A data phase is completed on any clock when both IRDY# and TRDY# are sampled asserted.
24	TRDY#	I/O	Target Ready This signal is driven low when the target is ready to complete the current data phase of the transaction. During a read, it indicates that valid data is asserted. During a write, it indicates that the target is prepared to accept data.
26	DEVSEL#	I/O	Device Select The DM9102H asserts the signal low when it recognizes its target address after FRAME# is asserted. As a bus master, the DM9102H will sample this signal which insures its destination address of the data transfer is recognized by a target.

27	STOP#	I/O	Stop This signal is asserted low by the target device to request the master device to stop the current transaction.
30	PERR#	I/O	Parity Error The DM9102H as a master or slave will assert this signal low to indicate a parity error on any incoming data.
31	SERR#	I/O	System Error This signal is asserted low when address parity is detected with enabled PCICS bit31 (detected parity error.) The system error asserts two clock cycles after the falling address if an address parity error is detected.
33	PAR	I/O	Parity This signal indicates even parity across AD0~AD31 and C/BE0#~C/BE3# including the PAR pin. This signal is an output for the master and an input for the slave device. It is stable and valid one clock after the address phase.
2,20,34,48	C/BE3# C/BE2# C/BE1# C/BE0#	I/O	Bus Command/Byte Enable During the address phase, these signals define the bus command or the type of bus transaction that will take place. During the data phase these pins indicate which byte lanes contain valid data. C/BE0# applies to bit7-0 and C/BE3# applies to bit31-24.
121,122,123,124,126,127, 128,1,6,7,10,11,13,14,16, 17,38,39,40,41,43,44,47, 49,50,51,54,55,56,57,59, 60	AD31~AD0	I/O	Address & Data or Boot ROM Address These are multiplexed address and data bus signals. As a bus master, the DM9102H will drive address during the first bus phase. During subsequent phases, the DM9102H will either read or write data expecting the target to increment its address pointer. As a target, the DM9102H will decode each address on the bus and respond if it is the target being addressed. AD17~AD0 can also be used as boot ROM address MA17~MA0 when the boot ROM is accessed.

5.2 Boot ROM and EEPROM Interfaces

Pin No. 128LQFP	Pin Name	I/O	Description
62	MD0/EEDI	I	Boot ROM Data Input/EEPROM Data In This is a multiplexed pin used by EEDI and MD0. When boot ROM is selected, it acts as boot ROM data input, otherwise the DM9102H will read the contents of EEPROM serially through this pin.
63,64,65,66,67,68,69	MD1~MD7	I	Boot ROM Data Input Bus MD1, MD2 and MD7 can be used as strap pins. See straps pin table for description.
72	BPCS#/EECS	O	Boot ROM (active low) or EEPROM Chip Selection.
78	EEDO	O	EEPROM Data Out This pin is used serially to write op-codes, addresses and data into the EEPROM.
79	EECK	O	EEPROM Serial Clock This pin is used as the clock for the EEPROM data transfer.

5.3 LED Pins

Pin No. 128LQFP	Pin Name	I/O	Description
75	IDSEL2	O	IDSEL2 When this pin pull-high, the PCI multiple function is present. And this pin act as PCI IDSEL 2 function.
83	GNT2#	O	GNT2# or LED Mode The DM9102H is in LED mode 1 when this pin is pulled high; otherwise the mode 0 is selected. When pin 75 is pull-high, the PCI multiple functions are present. And this pin act as PCI GNT2# function.
84	REQ2#	I	REQ2# When pin 75 is pull-high, the PCI multiple functions are present. And this pin act as PCI REQ2# function.
87	LINK&ACT# / ACT#	O	LED Output Pin, Active Low mode 0 = Link and traffic LED. Active low to indicate normal link and it will flash as traffic LED when transmitting or receiving. mode 1 = traffic LED only
88	FDX# / FDX#	O	LED Output Pin, Active Low mode 0 = Full duplex LED mode 1 = Full duplex LED
89	SPEED100# / SPEED100#	O	LED Output Pin, Active Low mode 0 = 100Mbps LED mode 1 = 100Mbps LED
90	SPEED10# / LINK#	O	LED Output Pin, Active Low mode 0 = 10Mbps LED mode 1 = Link LED

5.4 Network Interface

Pin No. 128LQFP	Pin Name	I/O	Description
105,106	RXI+ RX-	I	100M/10Mbps Differential Input Pair. These two pins are differential receive input pair for 100BASE-TX and 10BASE-T. They are capable of receiving 100BASE-TX MLT-3 or 10BASE-T Manchester encoded data.
109,110	TXO+ TXO-	O	100M/10Mbps differential output pair. These two pins are differential output pair for 100BASE-TX and 10BASE-T. This output pair provides controlled rising and falling time, designed to filter the transmitter's output.

5.5 Miscellaneous Pins

Pin No. 128LQFP	Pin Name	I/O	Description
36	CLOCKRUN#	I/O, O/D	Clockrun# The clockrun# signal is used by the system to pause or slow down the PCI clock signal. It is used by the DM9102H to enable or disable suspension of the PCI clock signal or restart of the PCI clock. When the clockrun# signal is not used, this pin should be connected to an external pulled down resistor.
71	TEST2	I	TEST mode control 2 In normal operation, this pin is pulled high.
37	TEST1	I	TEST Mode Control 1 In normal operation, this pin is pulled low.
94	WOL	O	Wake up signal. The DM9102H can assert this pin if it detects link status change, magic packet, or sample frame. The default is “normal low, active high pulse”. DM9102H also supports High/Low and Pulse/Level options.
97	X2	O	Crystal feedback output pin is used for crystal connection only. Leave this pin open if oscillator is used.
98	X1/OSC	I	Crystal or Oscillator Input. (25MHz±30ppm) 25MHz Oscillator or series resonance, fundamental frequency crystal.
102	BGRES	I	Band gap Voltage Reference Resistor. It connects to a 6.8KΩ1% error tolerance resistor between this pin and BGRESG pin, to provide an accurate current reference for DM9102H (10Base-T/100Base-TX Application).
101	BGRESG	I	For Band gap Circuit It is used together with the BGRES pin.
116	ISOLATE#	I	Isolate This isolate signal is used to isolate the DM9102H from the system, and it is suitable for LAN on motherboard. When isolate signal is active low, it disables the DM9102H function and the DM9102H will not drive any outputs and sample any inputs. In this case, the power consumption is minimum.
95	VCTRL18	O	Voltage 1.8V control This pin can be used to control a BJT transistor‘s base pin to generate a stable 1.8V power in BJT’s collect pin.

5.6 Power Pins

Pin No. 128LQFP	Pin Name	I/O	Description
99,100,107,108	AGND	P	Analog Ground
103,104,111,112	AVDD18	P	Analog Gower, +1.8V
8,9,15,22,28,29,35,37,45, 46,58,76,86,125	DGND	P	Digital Ground
82,120	DVDD18	P	Digital Power, +1.8V
4,5,12,18,19,25,32,42,52, 53,61,70,96	DVDD	P	Digital Power, +3.3V

5.7 NC Pins

Pin No. 128LQFP	Pin Name	I/O	Description
73,74,77,80,81,85,91,92,93	NC	-	These pins are unused in application and should let them unconnected.

6. Register Definition

6.1 PCI Configuration Registers

The definitions of PCI Configuration Registers are based on the PCI specification revision 2.2 and it provides the initialization and configuration information to operate the PCI interface in the DM9102H. All registers can be accessed with byte, word, or double word mode. As defined in PCI specification 2.1, read accesses to reserve or unimplemented registers will return a value of "0." These registers are to be described in the following sections.

The default value of PCI configuration registers after reset.

Description	Identifier	Address Offset	Value of Reset
Identification	PCIID	00H	91021282H
Command & Status	PCICS	04H	02100000H*
Revision	PCIRV	08H	02000060H
Miscellaneous	PCILT	0CH	BIOS determine
I/O Base Address	PCIIO	10H	System allocate
Memory Base Address	PCIMEM	14H	System allocate
Reserved	--------	18H - 28H	00000000H
Reserved	--------	24H	00000000H
Subsystem Identification	PCISID	2CH	load from SROM
Expansion ROM Base Address	PCIROM	30H	00000000H
Capability Pointer	CAP_PTR	34H	00000050H
Reserved	--------	38H	00000000H
Interrupt & Latency	PCIINT	3CH	System allocate bit7~0
Device Specific Configuration Register	PCIUSR	40H	00000000H**
Power Management Register	PCIPMR	50H	C0310001H**
Power Management Control & Status	PMCSR	54H	00000100H

* It is written to 02100007H by most BIOS.
** It may be changed from EEPROM in application.

Key to Default

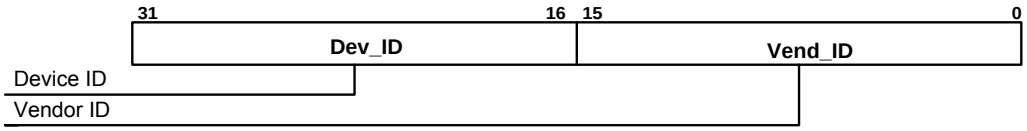
In the register description that follows, the default column takes the form <Reset Value>
Where：

<Reset Value>:

1	Bit set to logic one
0	Bit set to logic zero
X	No default value

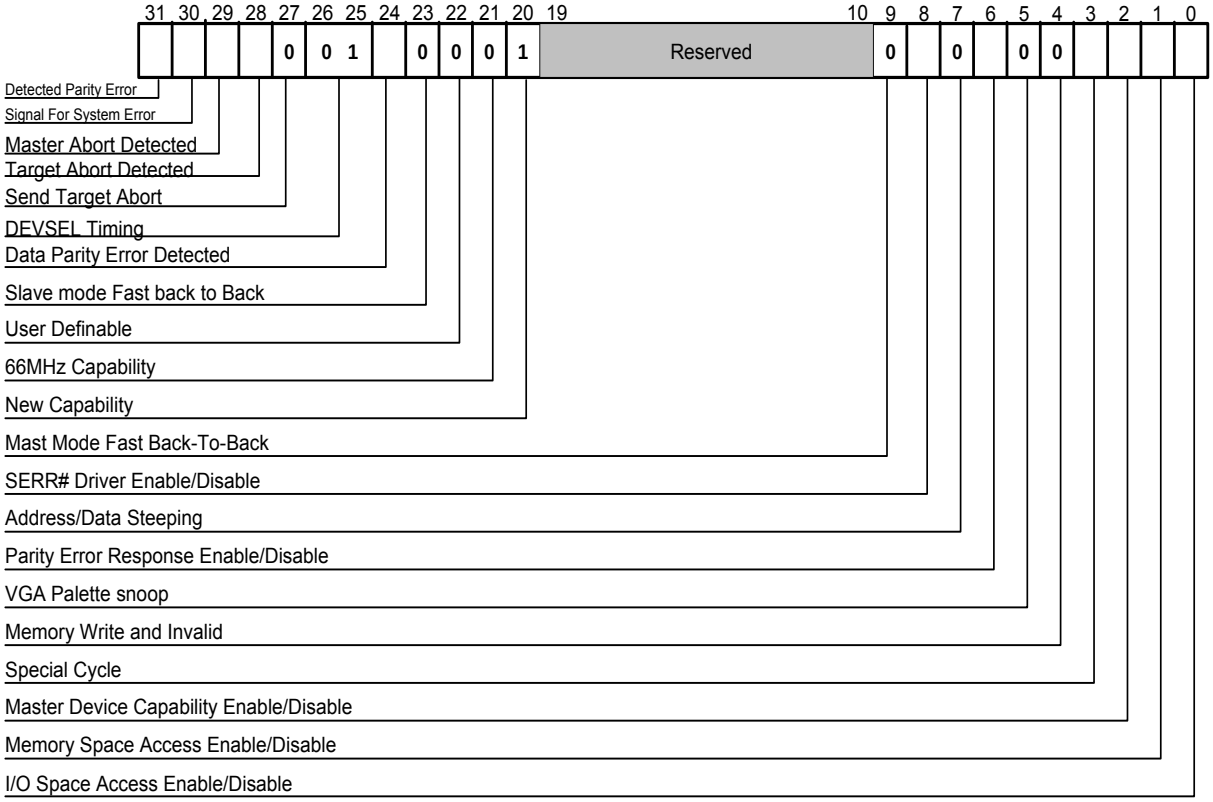
<Access Type>:
RO = Read only
RW = Read/Write
R/C: means Read / Write & Write "1" for Clear.

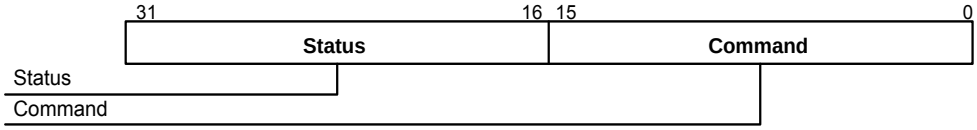
6.1.1 Identification ID (xxxxxx00H - PCIID)



Bit	Default	Type	Description
16:31	9102H	RO	The field identifies the particular device. Unique and fixed number for the DM9102H is 9102H. It is the product number assigned by DAVICOM
0:15	1282H	RO	This field identifies the manufacturer of the device. Unique and fixed number for Davicom is 1282H. It is a registered number from SIG

6.1.2 Command & Status (xxxxxx04H - PCICS)

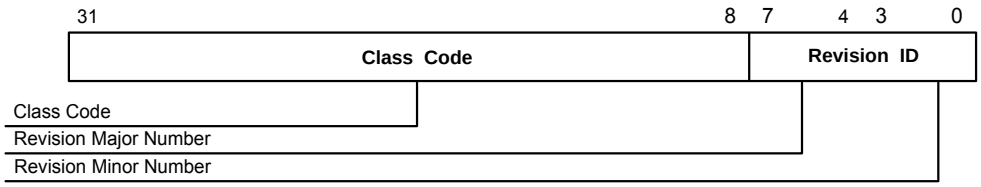




Bit	Default	Type	Description
31	0	R/C	Detected Parity Error The DM9102H samples the AD [0:31], C/BE [0:3] #, and the PAR signal to check parity and to set parity errors. In slave mode, the parity check falls on command phase and data valid phase (IRDY# and TRDY# both active). In master mode, the DM9102H will check each data phase, during a memory read cycle, for parity error. During a memory write cycle, if an error occurs, the PERR# signal will be driven by the target. This bit is set by the DM9102H and cleared by writing "1". There is no effect by writing "0"
30	0	R/C	Signal For System Error This bit is set when the SERR# signal is driven by the DM9102H. This system error occurs when an address parity is detected under the condition that bit 8 and bit 6 in command register below are set
29	0	R/C	Master Abort Detected This bit is set when the DM9102H terminates a master cycle with the master-abort bus transaction
28	0	R/C	Target Abort Detected This bit is set when the DM9102H terminates a master cycle due to a target-abort signal from other targets
27	0	R/C	Send Target Abort (0 for No Implementation) The DM9102H will never assert the target-abort sequence
26:25	01	R/C	DEVSEL Timing (01 Select Medium Timing) Medium timing of DEVSEL# means the DM9102H will assert DEVSEL# signal two clocks after FRAME# is sample “asserted”
24	0	R/C	Data Parity Error Detected This bit will take effect only when operating as a master and when a Parity Error Response Bit in command configuration register is set. It is set under two conditions: (i) PERR# asserted by the DM9102H in memory data read error (ii) PERR# sent from the target due to memory data write error
23	0	RO	Slave Mode Fast Back-To-Back Capable (0 for No Support) This bit is always reads "1" to indicate that the DM9102H is capable of accepting fast back-to-back transaction as a slave mode device
22	0	RO	User-Definable Feature Supported (0 for No Support)
21	0	RO	66 MHz (0 for No Capability)
20	1	RO	New Capability (1 For Good Capability) This bit indicates whether this function implements a list of extended capabilities such as PCI power management. When set this bit indicates the presence of New Capability. A value of 0 means that this function does not implement New Capability
19:10	0	RO	Reserved
9	0	RO	Master Mode Fast Back-To-Back (0 for No Support) The DM9102H does not support master mode fast back-to-back capability and will not generate fast back-to-back cycles
8	0	RW	SERR# Driver Enable/Disable This bit controls the assertion of SERR# signal output. The SERR# output

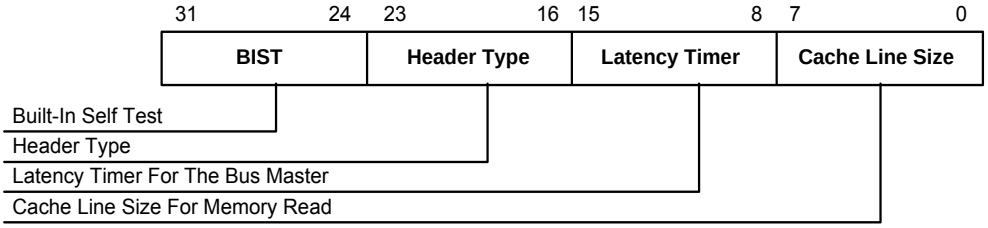
			will be asserted on detection of an address parity error and if both this bit and bit 6 are set
7	0	RO	Address/Data Stepping (0 for No Stepping)
6	0	RW	Parity Error Response Enable/Disable Setting this bit will enable the DM9102H to assert PERR# on the detection of a data parity error and to assert SERR# for reporting address parity error
5	0	RO	VGA Palette Snooping (0 for No Support)
4	0	RO	Memory Write and Invalid (0 for No Implementation) The DM9102H only generates memory write cycle
3	0	RO	Special Cycles (0 for No Implementation)
2	1	RW	Master Device Capability Enable/Disable When this bit is set, DM9102H has the ability of master mode operation
1	1	RW	Memory Space Access Enable/Disable This bit controls the ability of memory space access. The memory access includes memory mapped I/O access and Boot ROM access. As the system boots up, this bit will be enabled by BIOS for Boot ROM memory access. While in normal operation, using memory mapped I/O access, this bit should be set by driver before memory access cycles
0	1	RW	I/O Space Access Enable/Disable This bit controls the ability of I/O space access. It will be set by BIOS after power on

6.1.3 Revision ID (xxxxxx08H - PCIRV)



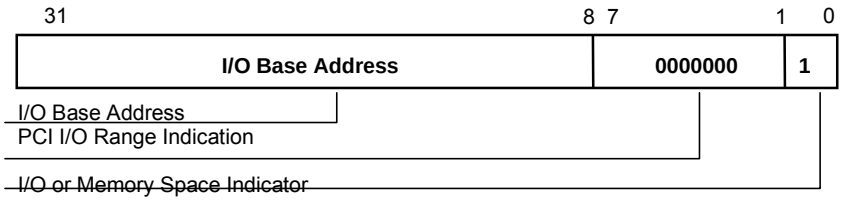
Bit	Default	Type	Description
31:8	020000H	RO	Class Code (020000H) This is the standard code for Ethernet LAN controller
7:4	0110	RO	Revision Major Number This is the silicon-major revision number that will increase for the subsequent versions of the DM9102H
3:0	0000	RO	Revision Minor Number This is the silicon-minor revision number that will increase for the subsequent versions of the DM9102H

6.1.4 Miscellaneous Function (xxxxxx0cH - PCILT)



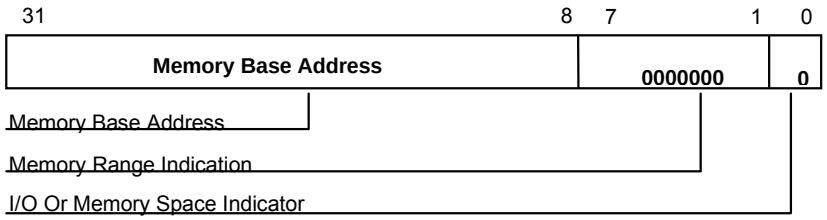
Bit	Default	Type	Description
31:24	00H	RO	Built In Self Test (00H means No Implementation)
23:16	00H	RO	Header Type (00H means single function with Predefined Header Type) If pin 75 is pull-high, header type is 80H means multiple functions are present.
15:8	00H	RW	Latency Timer For The Bus Master The latency timer is guaranteed by the system and measured by clock cycles. When the FRAME# is asserted at the beginning of a master period by the DM9102H, the value will be copied into a counter and start counting down. If the FRAME# is de-asserted prior to count expiration, this value is meaningless. When the count expires before GNT# is de-asserted, the master transaction will be terminated as soon as the GNT# is removed While GNT# signal is removed and the counter is non-zero, the DM9102H will continue with its data transfers until the count expires. The system host will read MIN_GNT and MAX_LAT registers to determine the latency requirement for the device and then initialize the latency timer with an appropriate value The reset value of Latency Timer is determined by BIOS
7:0	00H	RO	Cache Line Size For Memory Read Mode Selection (00H means No Implementation For Use)

6.1.5 I/O Base Address (xxxxxx10H - PCIIO)



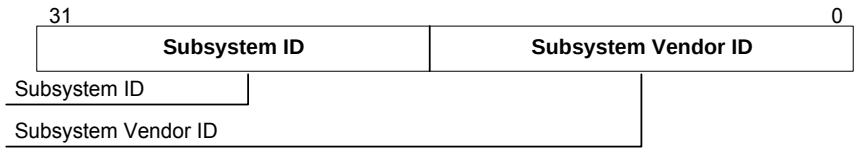
Bit	Default	Type	Description
31:7	Undefined	RW	PCI I/O Base Address This is the base address value for I/O accesses cycles. It will be compared to AD[31:7] in the address phase of bus command cycle for the I/O resource access
6:1	000000	RO	PCI I/O Range Indication It indicates that the minimum I/O resource size is 80h
0	1	RO	I/O Space Or Memory Space Base Indicator Determines that the register maps into the I/O space (= 1 Indicates I/O Base)

6.1.6 Memory Mapped Base Address (xxxxxx14H - PCIMEM)



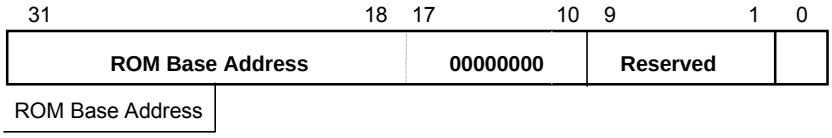
Bit	Default	Type	Description
31:7	Undefined	R/W	PCI Memory Base Address This is the base address value for memory accesses cycles. It will be compared to the AD [31:7] in the address phase of bus command cycle for the Memory resource access
6:1	000000	RO	PCI Memory Range Indication It indicates that the minimum memory resource size is 80h
0	0	RO	I/O Space Or Memory Space Base Indicator Determines that the register maps into the memory space(= 0 Indicates Memory Base)

6.1.7 Subsystem Identification (xxxxxx2cH - PCISID)



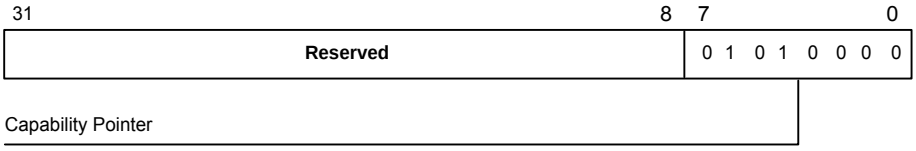
Bit	Default	Type	Description
31:16	XXXXH	RO	Subsystem ID It can be loaded from EEPROM word 1
15:0	XXXXH	RO	Subsystem Vendor ID Unique number given by PCI SIG and loaded from EEPROM word 0

6.1.8 Expansion ROM Base Address (xxxxxx30 - PCIROM)



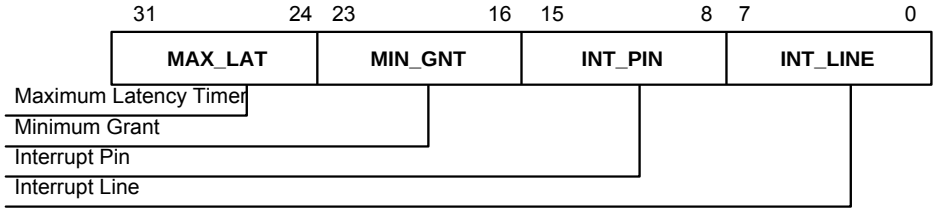
Bit	Default	Type	Description
31:10	00H	RW	ROM Base Address With 256K Boundary PCIROM bit17~10 are hardwired to 0, indicating ROM Size is up to 256K Size
9:1	000000000	RO	Reserved Bits Read As 0
0	0	RW	Expansion ROM Decoder Enable/Disable If this bit and the memory space access bit are both set to 1, the DM9102H will respond to its expansion ROM

6.1.9 Capabilities Pointer (xxxxxx34H - Cap_ Ptr)



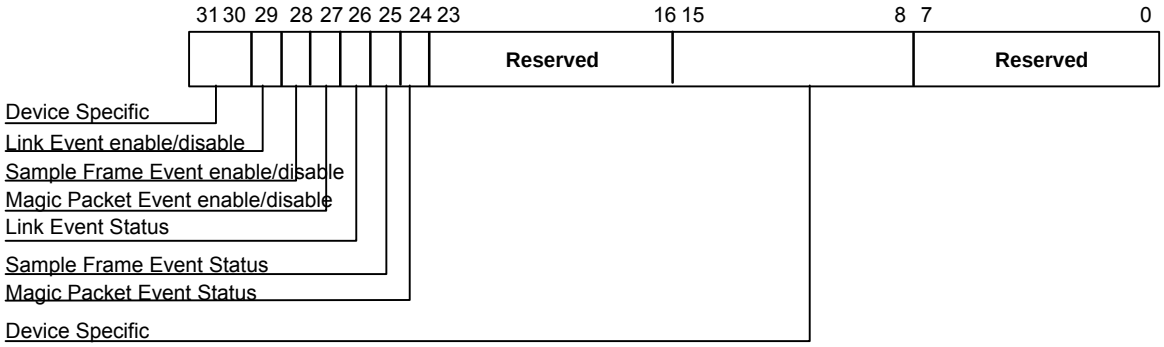
Bit	Default	Type	Description
31:8	000000H	RO	Reserved
7:0	01010000	RO	Capability Pointer The Cap_ Ptr provides an offset (default is 50H) into the function's PCI Configuration Space for the location of the first term in the Capabilities Linked List. The Cap_ Ptr offset is double word aligned so the two least significant bits are always "0"s

6.1.10 Interrupt & Latency Configuration (xxxxxx3cH - PCIINT)



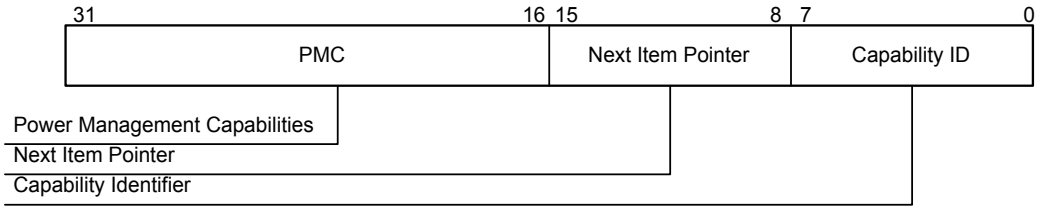
Bit	Default	Type	Description
31:24	28H	RO	Maximum Latency Timer that can be sustained (Read Only and Read As 28H)
23:16	14H	RO	Minimum Grant Minimum Length of a Burst Period (Read Only and Read As 14H)
15:8	01H	RO	Interrupt Pin read as 01H to indicate INTA#
7:0	XXH	RW	Interrupt Line that Is routed to the Interrupt Controller The value depends on main board

6.1.11 Device Specific Configuration Register (xxxxxx40H- PCIUSR)



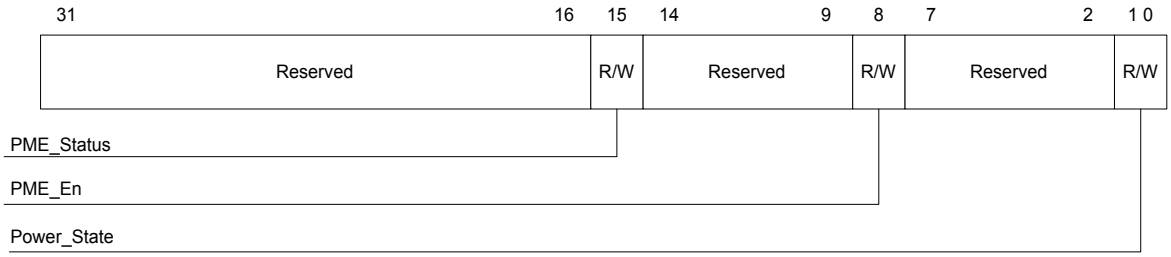
Bit	Default	Type	Description
31	0	RW	Device Specific Bit (sleep mode)
30	0	RW	Device Specific Bit (snooze mode)
29	0	RW	When set, enables Link Status Change Wake up Event
28	0	RW	When set, enables Sample Frame Wake up Event
27	0	RW	When set, enables Magic Packet Wake up Event
26	0	RO	When set, indicates the Link Change and the Link Status Change Event occurred
25	0	RO	When set, indicates the Sample Frame is received and the Sample Frame Event occurred
24	0	RO	When set, indicates the Magic Packet is received and the Magic packet Event occurred
23:16	00H	RO	Reserved Bits Read As 0
15:8	00H	RW	Device Specific
7:0	00H	RO	Reserved Bits Read As 0

6.1.12 Power Management Register (xxxxxx50H~PCIPMR)



Bit	Default	Type	Description
31:27	11000	RO	PME_ Support This field indicates that the power states in which the function may assert PME#. A value of 0 for any bit indicates that the function is not capable of asserting the PME# signal while in that power state bit27 → PME# support D0 bit28 → PME# support D1 bit29 → PME# support D2 bit30 → PME# support D3(hot) bit31 → PME# support D3(cold) DM9102H's bit31~27=11000 indicates PME# can be asserted from D3(hot) & D3(cold) These bits can be load from EEPROM word 7 bit [7:3]
26:25	00	RO	Reserved (DM9102H not supports D1, D2) These two bits can be load from EEPROM word 7 bit [1:0]
24:22	011	RO	Aux_ Current This field reports the 3.3Vaux auxiliary current requirement for the PCI function. The default value of this field is 011 means 160mA and it can be loaded from EEPROM word 4 bit [15:13] if EEPROM word 4 bit [9] is 1
21	1	RO	A "1" indicates that the function requires a device specific initialization sequence following transition to the D0 uninitialized state This bit can be load from EEPROM word 7 bit [2]
20	0	RO	Reserved
19	0	RO	PME# Clock "0" indicates that no PCI clock is required for the function to generate PME#
18:16	010	RO	Version A default value of 010 indicates that this function complies with the Revision 1.1 of the PCI Power Management Interface Specification This value can be loaded from EEPROM word 4 bit [12:10] if EEPROM word 4 bit [9] is 1
15:8	00H	RO	Next Item Pointer The offset into the function's PCI Configuration Space pointing to the location of next item in the function's capability list is "00H"
7:0	01H	RO	Capability Identifier When "01H" indicates the linked list item as being the PCI Power Management Registers

6.1.13 Power Management Control/Status (xxxxxx54H~PMCSR)



Bit	Default	Type	Description
31:16	0000H	RO	Reserved
15	0	RW/C	PME_ Status This bit is set when the function would normally assert the PME# signal independent of the state of the PME_ En bit. Writing a “1” to this bit will clear it. This bit defaults to “0” if the function does not support PME# generation from D3 (cold).If the function supports PME# from D3 (cold) then this bit is sticky and must be explicitly cleared by the operating system whenever the operating system is initially loaded
14:9	000000	RO	Reserved It means that the DM9102H does not support reporting power consumption
8	1	RW	PME_ En Write “1” to enables the function to assert PME#, write “0” to disable PME# assertion This bit defaults to “0” if the function does not support PME# generation from D3 (cold) If the function supports PME# from D3(cold) then this bit is sticky and must be explicitly cleared by the operating system each time the operating system is initially loaded
7:2	000000	RO	Reserved
1:0	00	RW	This two bits field is both used to determine the current power state of a function and to set the function into a new power state. The definitions given below 00: D0 11: D3 (hot)

6.2 Control and Status Registers (CR)

The DM9102H implements 16 control and status registers, which can be accessed by the host. These CRs are double long word aligned. All CRs are set to their default values by hardware or software reset unless otherwise specified. All Control and Status Registers with their definitions and offset from IO or memory Base Address are shown below:

Register	Description	Offset from CSR Base Address	Default value after reset
CR0	System Control Register	00H	DE000000H
CR1	Transmit Descriptor Poll Demand	08H	FFFFFFFFH
CR2	Receive Descriptor Poll Demand	10H	FFFFFFFFH
CR3	Receive Descriptor Base Address Register	18H	00000000H
CR4	Transmit Descriptor Base Address Register	20H	00000000H
CR5	Network Status Report Register	28H	FC000000H
CR6	Network Operation Mode Register	30H	02040000H
CR7	Interrupt Mask Register	38H	FFFE0000H
CR8	Statistical Counter Register	40H	00000000H
CR9	External Management Access Register	48H	000083F0H
CR10	Reserved	50H	FFFFFFFFH
CR11	Reserved	58H	FFFE0000H
CR12	PHY Status Register	60H	FFFFFFXXH
CR13	Sample Frame Access Register	68H	XXXXXX00H
CR14	Sample Frame Data Register	70H	Unpredictable
CR15	Watchdog And Jabber Timer Register	78H	00000000H

Key to Default

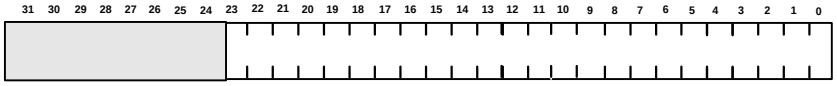
In the register description that follows, the default column takes the form:
<Reset Value>, <Access Type>
Where：
<Reset Value>:

1	Bit set to logic one
0	Bit set to logic zero
X	No default value

<Access Type>:
RO = Read only
RW = Read/Write
RW/C = Read/Write and Clear
WO = Write only

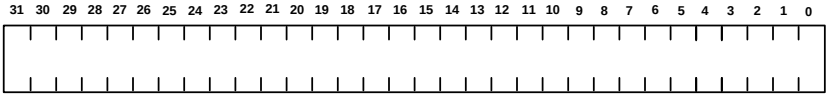
Reserved bits are shaded and should be written with 0.
Reserved bits are undefined on read access.

6.2.1 System Control Register (CR0)



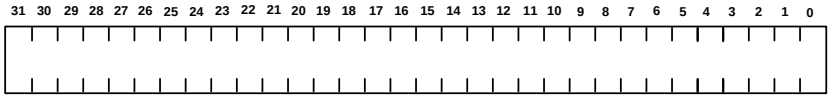
Bit	Name	Default	Description
31:26	Reserved	DEH,RO	Reserved
25:24	Reserved	00,RO	Reserved
23	TBURST	0,RW	TX DESC Burst Mode When set, PCI access TX DESC in burst mode
22	RBURST	0,RW	RX DESC Burst Mode When set, PCI access RX DESC in burst mode
21	MRM	0,RW	Memory Read Multiple When set, the DM9102H will use memory read multiple command (C/BE3~0 1100) when it initialize the memory read burst transaction as a master device When reset, it will use memory read command (C/BE3 ~ 0 = 0110) for the same master operation
20:1	Reserved	0,RO	Reserved
0	SR	0,RW	Software Reset When set, the DM9102H will make an internal reset cycle. All consequent action to DM9102H should wait at least 32 PCI clock cycles to start and no necessary to reset this bit

6.2.2 Transmit Descriptor Poll Demand (CR1)



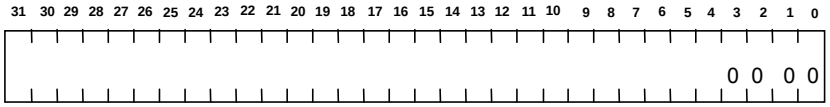
Bit	Name	Default	Description
31:0	TDP	FFFFFFFFH ,WO	Transmit Descriptor Polling Command Writing any value to this port will force DM9102H to poll the transmit descriptor. If the acting descriptor is not available, transmit process will return to suspend state. If the descriptor shows buffer available, transmit process will begin the data transfer

6.2.3 Receive Descriptor Poll Demand (CR2)



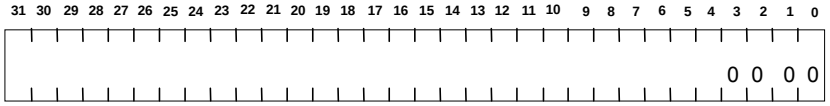
Bit	Name	Default	Description
31:0	RDP	FFFFFFFFH ,WO	Receive Descriptor Polling Command Writing any value to this port will force DM9102H to poll the receive descriptor. If the acting descriptor is not available, receive process will return to suspend state. If the descriptor shows buffer available, receive process will begin the data transfer

6.2.4 Receive Descriptor Base Address (CR3)



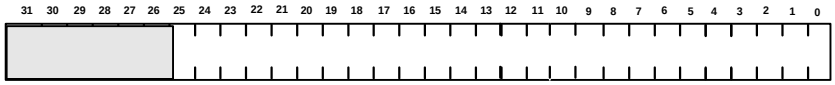
Bit	Name	Default	Description
31:0	RDBA	00000000H, RW	Receive Descriptor Base Address This register defines base address of receive descriptor-chain. The receive descriptor- polling command, after CR3 is set, will make DM9102H to fetch the descriptor at the Base-Address This is a working register, so the value of reading is unpredictable

6.2.5 Transmit Descriptor Base Address (CR4)



Bit	Name	Default	Description
31:0	TDBA	00000000H, RW	Transmit Descriptor Base Address This register defines base address of transmit descriptor-chain. The transmit descriptor- polling command after CR4 is set to make DM9102H fetch the descriptor at the Base-Address This is a working register, so the value of reading is unpredictable

6.2.6 Network Status Report Register (CR5)



Note: Bits [13:0] can be cleared by written 1 to them respectively.

Bit	Name	Default	Description
31:26	Reserved	000000,RO	Reserved
25:23	SBEB	000,RO	System Bus Error Bits These bits are read only and used to indicate the type of system bus fatal error. Valid only when System Bus Error is set. The mapping bits are shown below Bit25 Bit24 Bit23 Bus Error Type

			0 0 0 Parity error 0 0 1 Master abort 0 1 0 Slave abort 0 1 1 Reserved 1 X X Reserved
22:20	TXPS	000,RO	Transmit Process State These bits are read only and used to indicate the state of transmit process The mapping table is shown below Bit22 Bit21 Bit20 Process State 0 0 0 Transmit process stopped 0 0 1 Fetch transmit descriptor 0 1 0 Move Setup Frame from the host memory 0 1 1 Move data from host memory to transmit FIFO 1 0 0 Close descriptor by clearing owner bit of descriptor 1 0 1 Waiting end of transmit 1 1 0 Transmit end and Close descriptor by writing status 1 1 1 Transmit process suspend
19:17	RXPS	000,RO	Receive Process State These bits are read only and used to indicate the state of receive process. The mapping table is shown below Bit19 Bit18 Bit17 Process State 0 0 0 Receive process stopped 0 0 1 Fetch receive descriptor 0 1 0 Wait for receive packet under buffer available 0 1 1 Move data from receive FIFO to host memory 1 0 0 Close descriptor by clearing owner bit of descriptor 1 0 1 Close descriptor by writing status 1 1 0 Receive process suspended due to buffer unavailable 1 1 1 Purge the current frame from received FIFO because of the unavailable received buffer
16	NIS	0,RW	Normal Interrupt Summary Normal interrupt includes any of the three conditions: CR5<0> – TXCI: Transmit Complete Interrupt CR5<2> – TXDU: Transmit Buffer Unavailable CR5<6> – RXCI: Receive Complete Interrupt
15	AIS	0,RW	Abnormal Interrupt Summary Abnormal interrupt includes any interrupt condition as shown below, excluding Normal Interrupt conditions. They are TXPS (bit1), TXJT (bit3), TXFU (bit5), RXDU (bit7), RXPS (bit8), RXWT (bit9), SBE (bit13)
14	Reserved	0,RO	Reserved
13	SBE	0,RW	System Bus Error The PCI system bus errors will set this bit. The type of system bus error is shown in CR5<25:23>
12:10	Reserved	0,RO	Reserved
9	RXWT	0,RW	Receive Watchdog Timer Expired This bit is set to indicate that the receive watchdog timer has expired
8	RXPS	0,RW	Receive Process Stopped This bit is set to indicate that the receive process enters the stopped state
7	RXDU	0,RW	Receive Buffer Unavailable This bit is set when the DM9102H fetches the next receive descriptor that is still

			owned by the host. Receive process will be suspended until a new frame enters or the receive polling command is set
6	RXCI	0,RW	Receive Complete Interrupt This bit is set when a received frame is fully moved into host memory and receive status has been written to descriptor. Receive process is still running and continues to fetch next descriptor
5	TXFU	0,RW	Transmit FIFO Under run This bit is set when transmit FIFO has under run condition during the packet transmission. It may happen due to the heavy load on bus, receive process dominates in full-duplex operation, or transmit buffer unavailable before end of packet. In this case, transmit process is placed in the suspend state and under run error TDES0<1> is set
4	Reserved	0,RO	Reserved
3	TXJT	0,RW	Transmit Jabber Expired This bit is set when the transmitted data is over 2048 byte Transmit process will be aborted and placed in the stop state. It also causes transmit jabber timeout TDES0<14> to assert
2	TXDU	0,RW	Transmit Buffer Unavailable This bit is set when the DM9102H fetches the next transmit descriptor that is still owned by the host. Transmit process will be suspended until the transmission polling command is set or auto-polling timer time-out
1	TXPS	0,RW	Transmit Process Stopped This bit is set to indicate transmit process enters the stopped state
0	TXCI	0,RW	Transmit Complete Interrupt This bit is set when a frame is fully transmitted and transmit status has been written to descriptor (the TDES1<31> is also asserted). Transmit process is still running and continues to fetch next descriptor

6.2.7 Network Operation Mode Register (CR6)

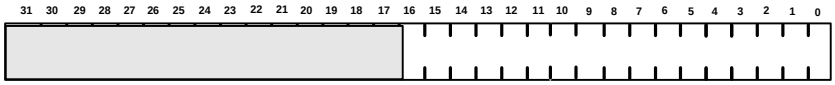
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			0	0	0	1	0	0					1	0	0								0			0					

Bit	Name	Default	Description
30	RXA	0,RW	Receive All When set, all incoming packet will be received, regardless the destination address. The address match is checked according to theCR6<7>, CR6<6>, CR6<4>, CR6<2>, CR6<0>, and RDES0<30> will show this match
29	NPFIFO	0,RW	Set to not purge RX FIFO if RX buffer unavailable
28:26	Reserved	000,RO	Must be Zero
25	Reserved	1,RO	Must be One
24:23	Reserved	00,RO	Must be Zero
22	TXTM	1,RW	Transmit Threshold Mode When set, the transmit threshold mode is 10Mb/s. When reset, the threshold mode is 100Mb/s. This bit is used together with CR6<15:14> to decide the exact threshold level

21	SFT	0,RW	Store and Forward Transmit When set, the packet transmission from MAC will be started after a full frame has been moved from the host memory to transmit FIFO. When reset, the packet transmission's start will depend on the threshold value specified in CR6<15:14>
20	Reserved	0,RW	Reserved
19	Reserved	0,RW	Reserved
18	External MII_ Mode	1,RW	In external MII mode, use this bit to enable or disable internal PHY 1: Select external MII interface See page 60 for details
17	RETRY	0,RW	TX Under-run Retry Mode When set, if transmit under run occurred, the transmit packet retried.
16	1PKT	0,RW	One Packet Mode When this bit is set, only one packet is stored at TX FIFO
15:14	TSB	0,RW	Threshold Bits These bits are set together with CR6 [22] and will decide the exact FIFO threshold level. The packet transmission will start after the data level exceeds the threshold value Bit 22 / Bit15 / Bit14 / Threshold 0 / 0 / 0 / 128 0 / 0 / 1 / 256 0 / 1 / 0 / 512 0 / 1 / 1 / 1024 1 / 0 / 0 / 64 1 / 0 / 1 / 128 1 / 1 / 0 / 192 1 / 1 / 1 / 256
13	TXSC	0,RW	Transmit Start/Stop Command When set, the transmit process will begin by fetching the transmit descriptor for available packet data to be transmitted (running state). If the fetched descriptor is owned by the host, transmit process will enter the suspend state and transmit buffer unavailable (CR5<2>) is set. Otherwise it will begin to move data from host to FIFO and transmit out after reaching threshold level When reset, the transmit process is placed in the stopped state after completing the transmission of the current frame
12	FCM	0,RW	Force Collision Mode When set, the transmission process is forced to be the collision status. Meaningful only in the internal Loopback mode
11:10	LBM	0,RW	Loopback Mode These bits decide two Loopback modes besides normal operation. External Loopback mode expects transmitted data back to receive path and makes no collision detection Bit11 / Bit10 / Loopback Mode 0 / 0 / Normal 0 / 1 / Internal Loopback 1 / 0 / Internal PHY digital Loopback 1 / 1 / Internal PHY analog Loopback

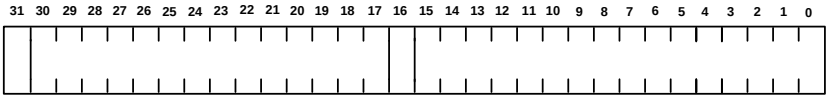
9	FDM	0,RW	Full-duplex Mode When internal PHY is selected, this bit is the status of full-duplex mode of internal PHY When external PHY is selected, set this bit to make the DM9102H operate in the full-duplex mode
8	Reserved	0,RO	Must be Zero
7	PAM	0,RW	Pass All Multicast When set, any packet with a multicast destination address is received by the DM9102H. The packet with a physical address will also be filtered based on the filter mode setting
6	PM	0,RW	Promiscuous Mode When set, any incoming valid frame is received by the DM9102H, and no matter what the destination address is. The DM9102H is initialized to this mode after reset operation
5:4	Reserved	0,RO	Must be Zero
3	PBF	0,RW	Pass Bad Frame When set, the DM9102 is indicated that receiving the bad frames, including runt packets and truncated frames, is caused by the FIFO overflow. The bad frame also has to pass the address filtering if the DM9102H is not set in promiscuous mode
2	HOFM	0,RO	Hash-only Filter Mode This is a read-only bit and mapped from the set-up frame together with bit4,0 of CR6 It is set to indicate the DM9102H operate in a Hash-only Filtering Mode
1	RXRC	0,RW	Receive Start/Stop Command When set, receive process will begin by fetching the receive descriptor for available buffer to store the new-coming packet (placed in the running state). If the fetched descriptor is owned by the host (no descriptor is owned by the DM9102H), the receive process will enter the suspend state and receive buffer unavailable CR5<7> sets. Otherwise it runs to wait for the packet's income. When reset, receive process is placed in the stopped state after completing the reception of the current frame
0	HPFM	0,RO	Hash/Perfect Filter Mode This is a read only bit and mapped from the setup frame together with CR6<4>, and CR6<2>. When reset, the DM9102H does a perfect address filter of incoming frames according to the addresses specified in the setup frame. When set, the DM9102H does an imperfect address filtering for the incoming frame with a multicast address according to the hash table specified in the setup frame. The filtering mode (perfect / imperfect) for the frame with a physical address will depend on CR6<2>.

6.2.8 Interrupt Mask Register (CR7)



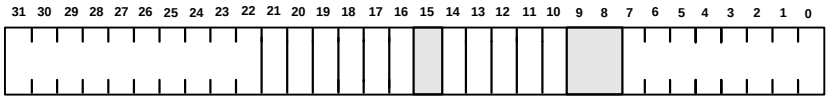
Bit	Name	Default	Description
16	NISE	0,RW	Normal Interrupt Summary Enable This bit is set to enable the interrupt for Normal Interrupt Summary. Normal interrupt includes three conditions: CR5<0> – TXCI: Transmit Complete Interrupt CR5<2> – TXDU: Transmit Buffer Unavailable CR5<6> – RXCI: Receive Complete Interrupt
15	AISE	0,RW	Abnormal Interrupt Summary Enable This bit is set to enable the interrupt for Abnormal Interrupt Summary. Abnormal interrupt includes all interrupt conditions as shown below, excluding Normal Interrupt conditions. They are TXPS (bit1), TXJT (bit3), TXFU (bit5), RXDU (bit7), RXPS (bit8), RXWT (bit9), SBE (bit13).
14	Reserved	0,RO	Reserved
13	SBEE	0,RW	System Bus Error Enable When set together with CR7<15>, CR5<13>, it enables the interrupt for System Bus Error. The type of system bus error is shown in CR5<24:23>.
12:10	Reserved	0,RO	Reserved
9	RXWTE	0,RW	Receive Watchdog Timer Expired Enable When this bit and CR7<15>, (CR5<9> are set together, it enable the interrupt of the condition of the receive watchdog timer expired.
8	RXPSE	0,RW	Receive Process Stopped Enable When set together with CR7<15> and CR5<8>. This bit is set to enable the interrupt of receive process stopped condition.
7	RXDUE	0,RW	Receive Buffer Unavailable Enable When this bit and CR7<15>, CR5<7> are set together, it will enable the interrupt of receive buffer unavailable condition.
6	RXCIE	0,RW	Receive Complete Interrupt Enable When this bit and CR7<16>, CR5<6> are set together, it will enable the interrupt of receive process complete condition.
5	TXFUE	0,RW	Transmit FIFO Under run Enable When set together with CR7<15>, CR5<5>, it will enable the interrupt of transmit FIFO under run condition.
4	Reserved	0,RO	Reserved
3	TXJTE	0,RW	Transmit Jabber Expired Enable When this bit and CR7<15>, CR5<3> are set together, it enables the interrupt of transmit Jabber Timer Expired condition.
2	TXDUE	0,RW	Transmit Buffer Unavailable Enable When this bit and CR7<16>, CR5<2> are set together, the interrupt of transmit buffer unavailable is enabled.
1	TXPSE	0,RW	Transmit Process Stopped Enable When this bit is set together with CR7<15> and CR5<1>, it will enable the interrupt of the transmit process to stop
0	TXCIE	0,RW	Transmit Complete Interrupt Enable When this bit and CR7<16>, CR5<0> are set, the transmit interrupt is enabled.

6.2.9 Statistical Counter Register (CR8)



Bit	Name	Default	Description
31	ROCO	0,RO	Receive Overflow Counter Overflow This bit is set when the Purged Packet Counter (RXDU) has an overflow condition. It is a read only register bit.
30:25	Reserved	0,RO	Reserved
24:17	RXDU	0,RO	Receive Purged Packet Counter This is a statistic counter to indicate the purged received packet counts upon FIFO overflow.
16	RXPS	0,RO	Receive Missed Counter Overflow This bit is set when the Receive Missed Frame Counter (RXCI) has an overflow condition. It is a read only register bit.
15:7	Reserved	0,RO	Reserved
6:0	RXCI	0,RO	Receive Missed Frame Counter This is a statistic counter to indicate the Receive Missed Frame Count when there is a host buffer unavailable condition for receive process.

6.2.10 Management Access Register (CR9)



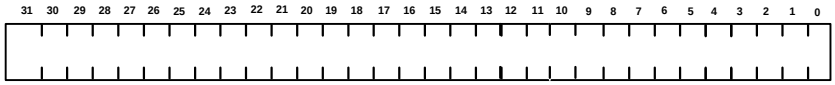
Bit	Name	Default	Description
31	MDIX	0,RO	Status of disable auto-MDIX function
30	MFUN	0,RO	Multi-function strap pin status
29	LEDM	0,RO	LED mode strap pin status
28:22	Reserved	X,RO	Reserved
21	LES	0,RO	Load EEPROM status It is set to indicate the load of EEPROM is finished.
20	RLM	0,RW	Reload EEPROM It is set to reload the content of EEPROM.
19	MDIN	0,RO	MII Management Data In This is a read-only bit to indicate the MDIO input data.
18	MRW	0,RW	MII Management Read/Write Mode Selection This bit defines the Read/Write Mode for MII management interface for PHY access. 1 for read.
17	MDOUT	0,RW	MII Management Data Out This bit is used to generate the output data signal for the MDIO pin.
16	MDCLK	0,RW	MII Management Clock This bit is used to generate the output clock signal for the MDC pin.

15	Reserved	1,RO	Reserved. Must be One.
14	Reserved	0,RO	Reserved
13	Reserved	0,RO	Reserved
12	Reserved	0,RW	Reserved
11	ERS	0,RW	EEPROM Selected This bit is set to select the EEPROM access for memory interface.
10	Reserved	1,RW	Reserved
9:8	Reserved	1,RO	Reserved. Must be One
7:4	Reserved	FH,RO	Reserved
3	CRDOUT	0,RW	Data Out from EEPROM This bit is set to reflect the signal status of EEDI pin when EEPROM mode is selected.
2	CRDIN	0,RW	Data In to EEPROM This bit is set to generate the output signal to EEDO pin when EEPROM mode is selected.
1	CRCLK	0,RW	Clock to EEPROM This bit is set to generate the output clock to EECLK pin when EEPROM mode is selected.
0	CRCS	0,RW	Chip Select to EEPROM This bit is set to generate the output signal to EECS pin when EEPROM mode is selected.

6.2.11 PHY Status Register (CR12)

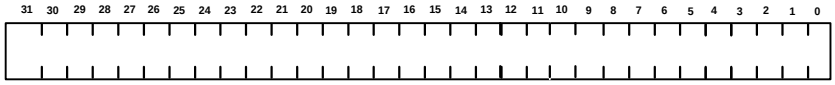
Bit	Name	Default	Description
31:9	Reserved	O	Reserved
8	GEPC	X,RW	GEPD Bits Control In initialization, this bit is set and the unique “80h” must be written to the GEPD (7:0). After initialization, this bit is reset and it controls the functional mode of GEPD in bit0~7.
7	GEPD(7)	X,RW	General PHY Reset Control It must be set to “1” if CR12<8> is set. When CR12<8> is reset, write “1” to this bit will reset the PHY of the DM9102H.
6:0	GEPD(6:0)	XXXXXXX ,RW	General PHY Status When CR12<8> is set at initialization, it operates the only write operation and write the unique “0000000” to these seven bits. After initialization, CR12<8> is reset, write operation is meaningless and read these seven bits to indicate the PHY status. These status bits are shown below. bit 6:Current Media Link Status bit 5:Signal Detection bit 4:RX-lock bit 3:Internal PHY Link status (the same as bit2 of PHY Register) bit 2:Full-duplex bit 1:Speed 100Mbps link bit 0:Speed 10Mbps link

6.2.12 Sample Frame Access Register (CR13) (reference to Power Management section)

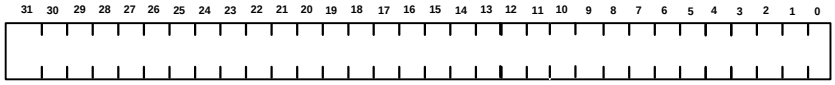


Register	General definition	bit8 ~ 3	R/W
TxFIFO	Transmit FIFO access port	32H	R/W
RxFIFO	Receive FIFO access port	35H	R/W
DiagReset	General reset for diagnostic pointer port	38H	W

6.2.13 Sample Frame Data Register (CR14) (reference to Power Management section)



6.2.14 Watchdog and Jabber Timer Register (CR15)



Bit	Name	Default	Description
31	TXSUMC	0,RW	In transmit; generate IP/TCP/UDP check sum depend-on TX desc. control
30	IPSUM	0,RW	In transmit; generate IP check sum to all packets
29	TCPSUM	0,RW	In transmit; generate TCP check sum to all packets
28	UDPSUM	0,RW	In transmit; generate UDP check sum to all packets
27	RXSUM	0,RW	In receiving; report IP/TCP/UDP checksum status to RDES0
26:16	Reserved	0,RO	Reserved
15	TXPM	0,RW	Transmit pause packet condition control 1 = Indicate Transmit pause packet either CR15<11> or CR15<12> is set. 0 = Indicate Transmit pause packet both CR15<11> and CR15<12> are set.
14	TXP0	0,RW	Transmit pause packet Set to Transmit pause packet with pause timer = 0000h, this bit will be cleared if packet had transmitted.
13	TXPF	0,RW	Transmit pause packet Set to Transmit pause packet with pause timer = FFFFh, this bit will be cleared if packet had transmitted.
12:11	Reserved	0,RO	Reserved
10	FLCE	0,RW	Flow Control Enable Set to enable the decode of the pause packet.
9	RXPS	0,R/C	The latched status of the decode of the pause packet.
8	Reserved	0,RO	Reserved.

7	RXPCS	0,RO	The decode of the pause packet.
6	VLAN	0,RW	VLAN length Capability Enable It is set to enable the VLAN length mode.
5	TWDR	0,RW	Time Interval of Watchdog Release This bit is used to select the time interval between receive Watchdog timer expiration until re-enabling of the receive channel. When this bit is set, the time interval is 40~48-bit time. When this bit is reset, it is 16~24 bits time.
4	TWDE	0,RW	Watchdog Timer Disable When set, the Watchdog Timer is disabled. Otherwise it is enabled.
3:1	Reserved	0,RO	Reserved
0	TJE	0,RW	Transmit Jabber Disable When set, the transmit Jabber is disabled. Otherwise it is enabled.

6.3 PHY Management Register Set

Offset	Register Name	Description	Default value after reset
0	BMCR	Basic Mode Control Register	3100H
1	BMSR	Basic Mode Status Register	7849H
2	PHYIDR1	PHY Identifier Register #1	0181H
3	PHYIDR2	PHY Identifier Register #2	B8B0H
4	ANAR	Auto-Negotiation Advertisement Register	01E1H
5	ANLPAR	Auto-Negotiation Link Partner Ability Register	0000H
6	ANER	Auto-Negotiation Expansion Register	0000H
7-15	Reserved	Reserved	0000H
10H	DSCR	DAVICOM Specified Configuration Register	0414H
11H	DSCSR	DAVICOM Specified Configuration/Status Register	F210H
12H	10BTCSR	10BASE-T Configuration/Status Register	7800H
Others	Reserved	Reserved for future use, do not read/write to these Registers	0000H

Key to Default

In the register description that follows, the default column takes the form:
<Reset Value>, <Access Type> / <Attribute(s)>
Where：

<Reset Value>:

1	Bit set to logic one
0	Bit set to logic zero
X	No default value
(PIN#)	Value latched in from pin # at reset

<Access Type>:
RO = Read only
RW = Read/Write

<Attribute (s)>:
SC = Self clearing
P = Value permanently set
LL = Latching low
LH = Latching high

6.3.1 Basic Mode Control Register (BMCR) – 0

Bit	Name	Default	Description
0.15	Reset	0, RW/SC	Reset: 1=Software reset 0=Normal operation This bit sets the status and controls the PHY registers of the DM9102H to their default states. This bit, which is self-clearing, will keep returning a value of one until the reset process is completed
0.14	Loopback	0, RW	Loopback: 1=Loop-back enabled 0=Normal operation When in 100Mbps operation mode, setting this bit may cause the descrambler to lose synchronization and produce a 720ms "dead time" before any valid data appear at the MII receive outputs
0.13	Speed Selection	1, RW	Speed Select: 1=100Mbps 0=10Mbps Link speed may be selected either by this bit or by Auto-negotiation. When Auto-negotiation is enabled and bit 12 is set, this bit will return Auto-negotiation selected media type.
0.12	Auto-negotiation Enable	1, RW	Auto-negotiation Enable: 1= Auto-negotiation enabled: bit 8 and 13 will be in Auto-negotiation status 0= Auto-negotiation disabled: bit 8 and 13 will determine the link speed and mode
0.11	Power Down	0, RW	Power Down: Setting this bit willpower down the whole chip except crystal / oscillator circuit. 1=Power Down 0=Normal Operation
0.10	Reserved	0,RO	Reserved. Write as 0, ignore on read.
0.9	Restart Auto-negotiation	0,RW/SC	Restart Auto-negotiation: 1= Restart Auto-negotiation. Re-initiates the Auto-negotiation process. When Auto-negotiation is disabled (bit 12 of this register cleared), this bit has no function and it should be cleared. This bit is self-clearing and it will keep returning a value of 1 until Auto-negotiation is initiated by the DM9102H. The operation of the Auto-negotiation process will not be affected by the management entity that clears this bit. 0= Normal Operation
0.8	Duplex Mode	1,RW	Duplex Mode: 1= Full Duplex operation. Duplex selection is allowed when Auto-negotiation is disabled (bit 12 of this register is cleared). With Auto-negotiation enabled, this bit reflects the duplex capability selected by Auto-negotiation. 0= Normal operation
0.7	Collision Test	0,RW	Collision Test: 1= Collision Test enabled. When set, this bit will cause the COL signal to be asserted in response to the assertion of TX_EN. 0= Normal Operation
0.6:0.0	Reserved	<0000000>, RO	Reserved. Write as 0, ignore on read

6.3.2 Basic Mode Status Register (BMSR) – 1

Bit	Name	Default	Description
1.15	100BASE-T4	0,RO/P	100BASE-T4 Capable: 1=DM9102H is able to perform in 100BASE-T4 mode 0=DM9102H is not able to perform in 100BASE-T4 mode
1.14	100BASE-TX Full Duplex	1,RO/P	100BASE-TX FULL DUPLEX CAPABLE: 1= DM9102H is able to perform 100BASE-TX in Full Duplex mode 0= DM9102H is not able to perform 100BASE-TX in Full Duplex mode
1.13	100BASE-TX Half Duplex	1,RO/P	100BASE-TX Half Duplex Capable: 1=DM9102H is able to perform 100BASE-TX in Half Duplex mode 0=DM9102H is not able to perform 100BASE-TX in Half Duplex mode
1.12	10BASE-T Full Duplex	1,RO/P	10BASE-T Full Duplex Capable: 1=DM9102H is able to perform 10BASE-T in Full Duplex mode 0=DM9102H is not able to perform 10BASE-T in Full Duplex mode
1.11	10BASE-T Half Duplex	1,RO/P	10BASE-T Half Duplex Capable: 1=DM9102H is able to perform 10BASE-T in Half Duplex mode 0=DM9102H is not able to perform 10BASE-T in Half Duplex mode
1.10-1.7	Reserved	0000,RO	Reserved: Write as 0, ignore on read
1.6	MF Preamble Suppression	1,RW	MII Frame Preamble Suppression: 1=PHY will accept management frames with preamble suppressed 0=PHY will not accept management frames with preamble suppressed
1.5	Auto-negotiation Complete	0,RO	Auto-negotiation Complete: 1=Auto-negotiation process completed 0=Auto-negotiation process not completed
1.4	Remote Fault	0,RO/LH	Remote Fault: 1= Remote fault condition detected (cleared on read or by a chip reset). Fault criteria and detection method is DM9102H specific implementation. This bit will set after the RF bit in the ANLPAR (bit 13, register address 05) is set 0= No remote fault condition detected
1.3	Auto-negotiation Ability	1,RO/P	Auto Configuration Ability: 1=DM9102H is able to perform Auto-negotiation 0=DM9102H is not able to perform Auto-negotiation
1.2	Link Status	0,RO/LL	Link Status: 1=Valid link established (for either 10Mbps or 100Mbps operation) 0=Link not established The link status bit is implemented with a latching function, so that the occurrence of a link failure condition causes the Link Status bit to be cleared and remain cleared until it is read via the management interface
1.1	Jabber Detect	0,RO/LH	Jabber Detect: 1=Jabber condition detected 0=No jabber This bit is implemented with a latching function. Jabber conditions will set this bit unless it is cleared by a read to this register through a management interface or a DM9102H reset. This bit works only in 10Mbps mode
1.0	Extended Capability	1,RO/P	Extended Capability: 1=Extended register capability 0=Basic register capability only

6.3.3 PHY Identifier Register #1 (PHYIDR1) – 2

The PHY Identifier Register#1 and Register#2 work together in a single identifier of the DM9102H. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), a vendor's model number, and a model revision number. DAVICOM Semiconductor's IEEE assigned OUI is 00606E.

Bit	Name	Default	Description
2.15-2.0	OUI_MSB	<0181H>, RO/P	OUI Most Significant Bits: This register stores bit 3 to 18 of the OUI (00606E) to bit 15 to 0 of this register respectively. The most significant two bits of the OUI are ignored (the IEEE standard refers to these as bit 1 and 2)

6.3.4 PHY Identifier Register #2 (PHYIDR2) - 3

Bit	Name	Default	Description
3.15-3.10	OUI_LSB	<101110>, RO/P	OUI Least Significant Bits: Bit 19 to 24 of the OUI (00606E) are mapped to bit 15 to 10 of this register respectively
3.9-3.4	VNDR_MDL	<001011>, RO/P	Vendor Model Number: Six bits of vendor model number mapped to bit 9 to 4 (most significant bit to bit 9)
3.3-3.0	MDL_REV	<0000>, RO/P	Model Revision Number: Four bits of vendor model revision number mapped to bit 3 to 0 (most significant bit to bit 3)

6.3.5 Auto-negotiation Advertisement Register (ANAR) – 4

This register contains the advertised abilities of this DM9102H device as they will be transmitted to its link partner during Auto-negotiation.

Bit	Name	Default	Description
4.15	NP	0,RO/P	Next Page Indication: 0=No next page available 1=Next page available The DM9102H has no next page, so this bit is permanently set to 0
4.14	ACK	0,RO	Acknowledge: 1=Link partner ability data reception acknowledged 0=Not acknowledged The DM9102H's Auto-negotiation state machine will automatically control this bit in the outgoing FLP bursts and set it at the appropriate time during the Auto-negotiation process. Software should not attempt to write to this bit.
4.13	RF	0, RW	Remote Fault: 1=Local Device senses a fault condition 0=No fault detected
4.12-4.11	Reserved	00, RW	Reserved: Write as 0, ignore on read
4.10	FCS	0, RW	Flow Control Support: 1=Controller chip supports flow control ability 0=Controller chip doesn't support flow control ability
4.9	T4	0, RW	100BASE-T4 Support: 1=100BASE-T4 supported by the local device

			0=100BASE-T4 not supported The DM9102H does not support 100BASE-T4 so this bit is 0 permanently
4.8	TX_FDX	1, RW	100BASE-TX Full Duplex Support: 1=100BASE-TX Full Duplex supported by the local device
4.7	TX_HDX	1, RW	100BASE-TX Support: 1=100BASE-TX supported by the local device 0=100BASE-TX not supported
4.6	10_FDX	1, RW	10BASE-T Full Duplex Support: 1=10BASE-T Full Duplex supported by the local device 0=10BASE-T Full Duplex not supported
4.5	10_HDX	1, RW	10BASE-T Support: 1=10BASE-T supported by the local device 0=10BASE-T not supported
4.4-4.0	Selector	<00001>, RW	Protocol Selection Bits: These bits contain the binary encoded protocol selector supported by this node. <00001> indicates that this device supports IEEE 802.3 CSMA/CD.

6.3.6 Auto-negotiation Link Partner Ability Register (ANLPAR) – 5

This register contains the advertised abilities of the link partner when received during Auto-negotiation.

Bit	Name	Default	Description
5.15	NP	0, RO	Next Page Indication: 1= Link partner, next page available 0= Link partner, no next page available
5.14	ACK	0, RO	Acknowledge: 1=Link partner ability data reception acknowledged 0=Not acknowledged The DM9102H's Auto-negotiation state machine will automatically control this bit from the incoming FLP bursts. Software should not attempt to write to this bit.
5.13	RF	0, RO	Remote Fault: 1=Remote fault is indicated by link partner 0=No remote fault is indicated by link partner
5.12-5.10	Reserved	000, RO	Reserved: Write as 0, ignore on read
5.9	T4	0, RO	100BASE-T4 Support: 1=100BASE-T4 is supported by the link partner 0=100BASE-T4 is not supported by the link partner
5.8	TX_FDX	0, RO	100BASE-TX Full Duplex Support: 1=100BASE-TX Full Duplex supported by the link partner 0=100BASE-TX Full Duplex not supported by the link partner
5.7	TX_HDX	0, RO	100BASE-TX Support: 1=100BASE-TX Half Duplex supported by the link partner 0=100BASE-TX Half Duplex not supported by the link partner
5.6	10_FDX	0, RO	10BASE-T Full Duplex Support: 1=10BASE-T Full Duplex supported by the link partner 0=10BASE-T Full Duplex not supported by the link partner
5.5	10_HDX	0, RO	10BASE-T Support: 1=10BASE-T Half Duplex supported by the link partner 0=10BASE-T Half Duplex not supported by the link partner
5.4-5.0	Selector	<00000>, RO	Protocol Selection Bits: Link partner's binary encoded protocol selector

6.3.7 Auto-negotiation Expansion Register (ANER) – 6

Bit	Name	Default	Description
6.15-6.5	Reserved	0, RO	Reserved: Write as 0, ignore on read
6.4	PDF	0, RO/LH	Local Device Parallel Detection Fault: PDF=1: A fault detected via parallel detection function. PDF=0: No fault detected via parallel detection function
6.3	LP_NP_ABLE	0, RO	Link Partner Next Page Able: LP_NP_ABLE=1: Link partner, next page available LP_NP_ABLE=0: Link partner, no next page
6.2	NP_ABLE	0,RO/P	Local Device Next Page Able: NP_ABLE=1: DM9102H, next page available NP_ABLE=0: DM9102H, no next page DM9102H does not support this function, so this bit is always 0.
6.1	PAGE_RX	0, RO/LH	New Page Received: A new link of code-word page received. This bit will be automatically cleared when the register (Register 6) is read by management
6.0	LP_AN_ABLE	0, RO	Link Partner Auto-negotiation Able: A "1" in this bit indicates that the link partner supports Auto-negotiation.

6.3.8 DAVICOM Specified Configuration Register (DSCR) – 10H

Bit	Name	Default	Description
16.15:16.10	Reserved	000001,RW	Reserved
16.9:16.8	Reserved	00, RO	Reserved
16.7	F_LINK_100	0, RW	Force Good Link in 100Mbps: 1 = Force 100Mbps good link status 0 = Normal 100Mbps operation This bit is useful for diagnostic purposes.
16.6:16.5	Reserved	00,RW	Reserved
16.4	RPDCTR_EN	1,RW	Reduced Power Down Control Mode: This bit is used to enable automatic reduced power down 1 = Enable automatic reduced power down 0 = Disable automatic reduced power down
16.3	SMRST	0,RW	Reset State Machine: When writes 1 to this bit, all state machines of PHY will be reset. This bit is self-clear after reset is completed.
16.2	MFPSC	1,RW	MF Preamble Suppression Control: MII frame preamble suppression control bit 1 = MF preamble suppression bit on 0 = MF preamble suppression bit off
16.1	SLEEP	0,RW	Sleep Mode: Writing a 1 to this bit will cause PHY entering the Sleep mode and power down all circuit except oscillator and clock generator circuit. When waking up from Sleep mode (write this bit to 0), the configuration will go back to the state before sleep; but the state machine will be reset
16.0	RLOUT	0,RW	Remote Loop out Control: When this bit is set to 1, the received data will loop out to the transmit channel. This is useful for testing bit error rate

6.3.9 DAVICOM Specified Configuration and Status Register (DSCSR) – 11H

Bit	Name	Default	Description
17.15	100FDX	1, RO	100M Full Duplex Operation Mode: After Auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 100Mbps Full Duplex mode. The software can read bit [15:12] to see which mode is selected after Auto-negotiation. This bit is invalid when it is not in the Auto-negotiation mode.
17.14	100HDX	1, RO	100M Half Duplex Operation Mode: After Auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 100Mbps Half Duplex mode. The software can read bit [15:12] to see which mode is selected after Auto-negotiation. This bit is invalid when it is not in the Auto-negotiation mode.
17.13	10FDX	1, RO	10M Full Duplex Operation Mode: After Auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 10Mbps Full Duplex mode. The software can read bit [15:12] to see which mode is selected after Auto-negotiation. This bit is invalid when it is not in the Auto-negotiation mode.
17.12	10HDX	1, RO	10M Half Duplex Operation Mode: After Auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 10Mbps Half Duplex mode. The software can read bit [15:12] to see which mode is selected after Auto-negotiation. This bit is invalid when it is not in the Auto-negotiation mode.
17.11-17.10	Reserved	00, RO	Reserved:
17.9	Reserved	1, RW	Reserved: Write as 0, ignore on read
17.8-17.4	PHYAD[4:0]	00001, RW	PHY Address Bit 4:0: The first PHY address bit transmitted or received is the MSB of the address (bit 4). A station management entity connected to multiple PHY entities must know the appropriate address of each PHY. A PHY address of <00000> will cause the isolate bit of the BMCR (bit 10, Register Address 00) to be set.
17.3-17.0	ANMB[3:0]	0000, RO	Auto-negotiation Monitor Bits: These bits are for debug only. The Auto-negotiation status will be written to these bits. . . . .

b3	b2	b1	b0	
0	0	0	0	In IDLE state
0	0	0	0	Ability match
0	0	1	0	Acknowledge match
0	0	1	1	Acknowledge match fail
0	1	0	0	Consistency match
0	1	0	1	Consistency match fail
0	1	1	0	Parallel detects signal_link_ready
0	1	1	1	Parallel detects signal_link_ready fail
1	0	0	0	Auto-negotiation completed successfully

6.3.10 10BASE-T Configuration/Status (10BTCSRCSR) – 12H

Bit	Name	Default	Description
18.15	Reserved	0, RO	Reserved: Write as 0, ignore on read
18.14	LP_EN	1, RW	Link Pulse Enable: 1=Transmission of link pulses enabled 0=Link pulses disabled, good link condition forced This bit is valid only in 10Mbps operation.
18.13	HBE	1,RW	Heartbeat Enable: 1=Heartbeat function enabled 0=Heartbeat function disabled When the DM9102H is configured for Full Duplex operation, this bit will be ignored (the collision/heartbeat function is invalid in Full Duplex mode). It must set to be 1.
18.12	SQUELCH	1, RW	Squelch Enable 1 = normal squelch 0 = low squelch
18.11	JABEN	1, RW	Jabber Enable: Enables or disables the Jabber function when the DM9102H is in 10BASE-T Full Duplex or 10BASE-T Transceiver Loopback mode 1= Jabber function enabled 0= Jabber function disabled
18.10	Reserved	0,RW	Reserved
18.9-18.2	Reserved	0, RO	Reserved
18.1	Reserved	1,RW	Reserved
18.0	POLR	0, RO	Polarity Reversed When this bit is set to 1, it indicates that the 10Mbps cable polarity is reversed. This bit is automatically set and cleared by 10BASE-T module

6.3.11 Power down Control Register (PWDOR) – 13H

Bit	Bit Name	Default	Description
19.15-19.9	Reserved	0, RO	Reserved Read as 0, ignore on write
19.8	PD10DRV	0, RW	Vendor power down control test
19.7	PD100DL	0, RW	Vendor power down control test
19.6	PDchip	0, RW	Vendor power down control test
19.5	PDcom	0, RW	Vendor power down control test
19.4	PDaeq	0, RW	Vendor power down control test
19.3	PDdrv	0, RW	Vendor power down control test
19.2	PDedi	0, RW	Vendor power down control test
19.1	PDedo	0, RW	Vendor power down control test
19.0	PD10	0, RW	Vendor power down control test

***** When selected, the power down value is control by Register 20.0

6.3.12 (Specified config) Register – 20

Bit	Bit Name	Default	Description
20.15	TSTSE1	0,RW	Vendor test select control
20.14	TSTSE2	0,RW	Vendor test select control
20.13	FORCE_TXSD	0,RW	Force Signal Detect 1: force SD signal OK in 100M 0: normal SD signal.
20.12	TSTSEL3	0,RW	Vendor test select control
20.11	PREAMBLEX	0,RW	Preamble Saving Control 1: when bit 10 is set, the 10M TX preamble count is reduced. When bit 11 of register 29 is set, 10-bit preamble bit is reduced; otherwise a 5-bit preamble bit is reduced. 0: 10M TX preamble bit count is normal.
20.10	TX10M_PWR	0,RW	10M TX Power Saving Control 1: enable 10M TX power saving 0: disable 10M TX power saving
20.9	NWAY_PWR	0,RW	N-Way Power Saving Control 1: disable N-Way power saving 0: enable N-Way power saving
20.8	Reserved	0, RO	Reserved Read as 0, ignore on write
20.7	MDIX_CNTL	MDI/MDIX,RO	The polarity of MDI/MDIX value 1: MDIX mode 0: MDI mode
20.6	AutoNeg_dpbk	0,RW	Auto-negotiation Loopback 1: test internal digital auto-negotiation Loopback 0: normal.
20.5	Mdix_fix Value	0, RW	MDIX_CNTL force value: When MDIX_DOWN = 1, MDIX_CNTL value depend on the register value.
20.4	Mdix_do wn	0,RW	MDIX Down Manual force MDI/MDIX. 0: Enable HP Auto-MDIX 1: Disable HP Auto-MDIX , MDIX_CNTL value depend on 20.5
20.3	MonSel1	0,RW	Vendor monitor select
20.2	MonSel0	0,RW	Vendor monitor select
20.1	RMII_Ver	0,RW	RMII version 0: support RMII 1.2 1: support RMII 1.0
20.0	PD_value	0,RW	Power down control value Decision the value of each field Register 19. 1: power down 0: normal

6.3.13 Power Saving Control Register (PSCR) – 1DH

Bit	Bit Name	Default	Description
29.15-12	RESERVED	0,RO	reserved
29.11	PREAMBLEX	0,RW	Preamble Saving Control When both bit 10and 11 of register 20 are set, the 10M TX preamble count is reduced. 1: 10-bit preamble bit is reduced. 0: A 5-bit preamble bit is reduced.
29.10	AMPLITUDE	0,RW	10M TX Amplitude Control Disabled 0: when cable is unconnected with link partner, the TX amplitude is reduced for power saving. 1: disable TX amplitude reduce function
29.9	TX_PWR	0.RW	TX Power Saving Control Disabled 0: when cable is unconnected with link partner, the driving current of transmit is reduced for power saving. 1: disable TX driving power saving function
29.8-0	RESERVED	0,RO	reserved

7. Functional Description

7.1 System Buffer Management

7.1.1 Overview

The data buffers for reception and the transmission of data reside in the host memory. They are directed by the descriptor list that is located in another region of the host memory. All actions for the buffer management are operated by the DM9102H in conjunction with the driver. The data structures and processing algorithms are described in the following text.

7.1.2 Data Structure and Descriptor List

There are two types of buffers that reside in the host memory, the transmit buffer and the receive buffer. The buffers are composed of many distributed regions in the host memory. They are linked together and controlled by the descriptor lists that reside in another region of the host memory. The descriptor list is a Chain structure. The content of each descriptor includes pointer to the buffer, count of the buffer, command and status for the packet to be transmitted or received. Each descriptor list starts from the address setting of CR3 (receive descriptor base address) and CR4 (transmit descriptor base address). Refer to Figure 7-1.

7.1.3 Buffer Management -- Chain Structure Method

As the Chain structure depicted below, each descriptor contains two pointers, one point to a single buffer and the other to the next descriptor chained. The first descriptor is chained to the last descriptor under host driver's control. With this structure, a descriptor can be allocated anywhere in host memory and is chained to the next descriptor.

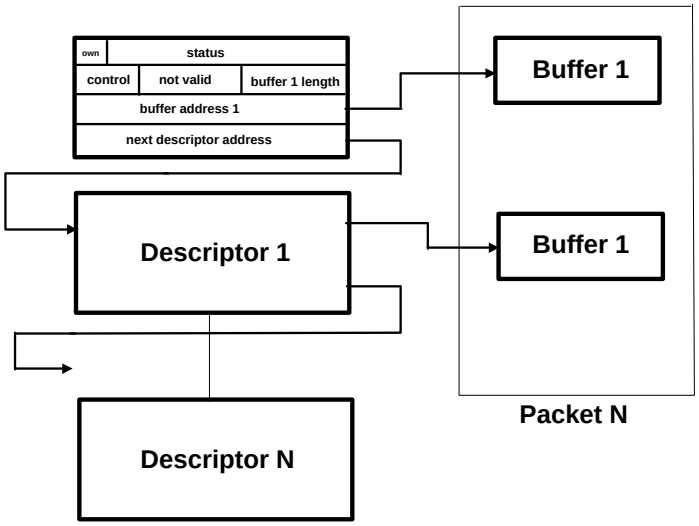


Figure 7-1

7.1.4 Descriptor List: Buffer Descriptor Format

(a). Receive Descriptor Format

Each receive descriptor has four double word entries and may be read or written by the host or the DM9102H. The descriptor format is shown below with a detailed functional description.

31		0	
OWN	Status		RDES 0
Control bits		Buffer Length	RDES 1
Buffer Address			RDES 2
Next Descriptor Address			RDES 3

Receive Descriptor Format

RDES0:

31	30	29 28 27 26 25 24 23 22 21 20 19 18 17 16
OWN	AUN	Frame Length (FL)

OWN: Owner bit of received status
1=owned by DM9102, 0=owned by host
This bit should be reset after packet reception is completed. The host will set this bit after received data is removed.

AUN: Received address unmatched.

FL: Frame Length
Frame length indicates total byte count of received packet.

15	14	13 12	11	10	9	8	7	6	5	4	3	2	1	0
ES	DUE	LBOM	RF	MF	BD	ED	EFL	LCS	FT	RWT	PLE	AE	CE	FOE

This word-wide content includes status of received frame. They are loaded after the received buffer that belongs to the corresponding descriptor is full. All status bits are valid only when the last descriptor (End Descriptor) bit is set.

Bit 15: ES, Error Summary
It is set for the following error conditions:
Descriptor Unavailable Error (DUE =1), Runt Frame (RF=1), Excessive Frame Length (EFL=1), Late Collision Seen (LCS=1), CRC error (CE=1), FIFO Overflow error (FOE=1). Valid only when ED is set.

Bit 14: DUE, Descriptor Unavailable Error
It is set when the frame is truncated due to the buffer unavailable. It is valid only when ED is set.

Bit 13, 12: LBOM, Loopback Operation Mode or IP/TCP/UDP checksum status
If CR15 bit 27 is set, these two bits present the IP/TCP/UDP status:
0X -- IP checksum OK
1X --IP checksum FAIL
X0 – TCP or UDP checksum OK
X1 – TCP or UDP checksum FAIL
; Otherwise
These two bits show the received frame is derived from:
00 --- Normal
01 --- Internal Loopback
10 --- Internal PHY digital Loopback
11 --- Internal PHY analog Loopback

Bit 11: RF, Runt Frame

It is set to indicate the received frame has the size smaller than 64 bytes. It is valid only when ED is set and FOE is reset.

Bit 10: MF, Multicast Frame
It is set to indicate the received frame has a multicast address. It is valid only when ED is set.

Bit 9: BD, Begin Descriptor
This bit is set for the descriptor indicating the start of a received frame.

Bit 8: ED, End Descriptor
This bit is set for descriptor to indicate the end of a received frame.

Bit 7: EFL, Excessive Frame Length
It is set to indicate the received frame length exceeds 1518 bytes. Valid only when ED is set.

Bit 6: LCS: Late Collision Seen
It is set to indicate a late collision found during the frame reception. Valid only when ED is set.

Bit 5: FT, Frame Type or IP packet
If CR15 bit 27 is set, this bit present the flag that this is IP packet; otherwise
It is set to indicate the received frame is the Ethernet-type. It is reset to indicate that the received frame is the EEE802.3-type. Valid only when ED is set

Bit 4: RWT, Receive Watchdog Time-Out or TCP packet
If CR15 bit 27 is set, this bit present the flag that this is TCP packet; otherwise
It is set to indicate the received watchdog time-out during the frame reception. CR5<9> will also be set. Valid only when ED is set.

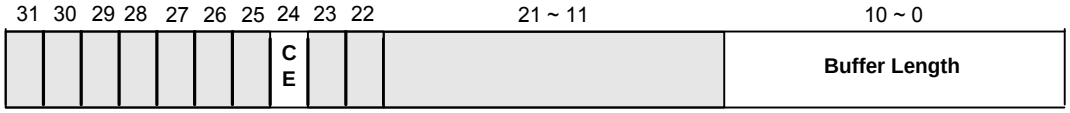
Bit 3: PLE, Physical Layer Error or UDP packet
If CR15 bit 27 is set, this bit present the flag that this is UDP packet; otherwise
It is set to indicate a physical layer error found during the frame reception.

Bit 2: AE, Alignment Error
It is set to indicate the received frame ends with a non-byte boundary.

Bit 1: CE, CRC Error
It is set to indicate the received frame ends with a CRC error. Valid only when ED is set.

Bit 0: FOE, FIFO Overflow Error
This bit is valid only when End Descriptor is set. (ED = 1). It is set to indicate a FIFO overflow error happens during the frame reception.

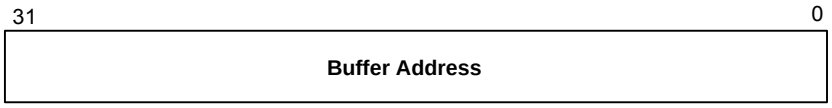
RDES1: Descriptor Status and Buffer Size



Bit 24: Must be 1.

Bit 10-0: Buffer Length
Indicates the size of the buffer.

RDES2: Buffer Starting Address
Indicates the physical starting address of buffer. This address must be double word aligned.



RDES3: Next descriptor Address
Indicates the physical starting address of the chained descriptor under the Chain descriptor structure.
This address must be eight-word aligned.

31	0
Next descriptor Address	

(b). Transmit Descriptor Format

Each transmit descriptor has four double word content and may be read or written by the host or by the DM9102H. The descriptor format is shown below with detailed description

31			0	
OWN	Status			TDES0
Control bits		Buffer Length		TDES1
Buffer Address				TDES2
Next Descriptor Address				TDES3

Transmit Descriptor Format

TDES0: Owner Bit with Transmit Status

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OWN															

Bit 31: OWN,
1=owned by DM9102H, 0=owned by host, this bit should be set when the transmitting buffer is filled with data and ready To be transmitted. It will be reset by DM9102H after transmitting the whole data buffer.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ES	TX JT			LOC	NC	LC	EC	0	CC				0	FUE	DF

This word wide content includes status of transmitted frame. They are loaded after the data buffer that belongs to the corresponding descriptor is transmitted.

Bit 15: ES, Error Summary
It is set for the following error conditions:

Transmit Jabber Time-out (TXJT=1), Loss of Carrier (LOC=1), No Carrier (NC=1), Late Collision (LC=1), Excessive Collision (EC=1), FIFO Under run Error (FUE=1).

Bit 14: TXJT, Transmit Jabber Time Out

It is set to indicate the transmitted frame is truncated due to transmit jabber time out condition. The transmit jabber time out interrupt CR5<3> is set.

Bit 12: TX had been under run
It is set to indicate the transmit had been under run occurred.

Bit 11: LOC, Loss of Carrier
It is set to indicate the loss of carrier during the frame transmission. It is not valid in internal Loopback mode.

Bit 10: NC, No Carrier
It is set to indicate that no carrier signal from transceiver is found. It is not valid in internal Loopback mode.

Bit 9: LC, Late Collision
It is set to indicate a collision occurs after the collision window of 64 bytes. Not valid if FUE is set.

Bit 8: EC, Excessive collision
It is set to indicate that the transmission is aborted due to 16 excessive collisions.

Bit 7: Reserved
This bit is 0 when read.

Bits 6-3: CC, Collision Count
These bits show the number of collision before transmission. Not valid if excessive collision bit is also set.

Bit 2: Reserved
This bit is 0 when read.

Bit 1: FUE, FIFO under run Error
It is set to indicate that the transmission aborted due to transmit FIFO under run condition.

Bit 0: DF, Deferred
It is set to indicate that the frame is deferred before ready to transmit.

TDES1: Transmit buffer control and buffer size

31	30	29	28	27	26	25	24	23	22	21 ~ 11	10 ~ 0
CI	ED	BD	FMB1	SETF	CAD	///	CE	PD	FMB0		Buffer Length

Bit 31: CI, Completion Interrupt
It is set to enable transmit interrupt after the present frame has been transmitted. It is valid only when TDES1<30> is set or when it is a setup frame.

Bit 30: ED, Ending Descriptor
It is set to indicate the pointed buffer contains the last segment of a frame.

Bit 29: BD, Begin Descriptor
It is set to indicate the pointed buffer contains the first segment of a frame.

Bit 28: FMB1, Filtering Mode Bit 1
This bit is used with FMB0 to indicate the filtering type when the present frame is a setup frame.

Bit 27: SETF, Setup Frame
It is set to indicate the current frame is a setup frame.
(Refer to 7.1.5 Setup Frame)

Bit 26: CAD, CRC Append Disable
It is set to disable the CRC appending at the end of the transmitted frame. Valid only when TDES1<29> is set.

Bit 24: CE, Chain Enable
Must be “1”.

Bit 23: PD, Padding Disable
This bit is set to disable the padding field for a packet shorter than 64 bytes.

Bit 22: FMB0, Filtering Mode Bit 0
This bit is used with FMB1 to indicate the filtering type when the present frame is a setup frame.

FMB1	FMB0	Filtering Type
0	0	Perfect Filtering
0	1	Hash Filtering
1	0	Inverse Filtering
1	1	Hash-Only Filtering.

Bit 21: IP Packet Checksum Generation
This bit is set to enable the IP packet checksum generation, if per-packet checksum in CR15 bit 31 is enabled

Bit 20: TCP Packet Checksum Generation
This bit is set to enable the TCP packet checksum generation, if per-packet checksum in CR15 bit 31 is enabled.

Bit 19: UDP Packet Checksum Generation
This bit is set to enable the UDP packet checksum generation, if per-packet checksum in CR15 bit 31 is enabled.

Bit 10-0: Buffer 1 length
Indicates the size of buffer in Chain type structure.

TDES2: Buffer Starting Address indicates the physical starting address of buffer.

31	0
Buffer Address 1	

TDES3: Address indicates the next descriptor starting address
Indicates the physical starting address of the chained descriptor under the Chain descriptor structure.
This address must be eight-word alignment.

31	0
Buffer Address 2	

7.1.5 Setup Frame

A setup frame fills the DM9102H Ethernet address table. The setup frame would not be transmitted on the Ethernet wire nor is it looped back to the receive list. When DM9102H is handling the setup frame, the receiver of DM9102H will stop to operate from the Ethernet wire till DM9102H has finished the setup frame handling. The address table uses double-word unit (four bytes). The DM9102H just use low word to fill Ethernet address, thus an Ethernet address needs three words. An Ethernet address has 6 bytes and DM9102H needs to keep 16 Ethernet addresses, thus DM9102H needs 96 bytes to save the information. In other words, the setup frame size must be exactly192 bytes. The following section will describe four modes of setup frame.

Note: The setup frame must be allocated in a single buffer that is long word aligned. First segment (TDES1<29>) and last segment (TDES1<30>) must both be 0. When the setup frame load is completed, the DM9102H closes the setup frame descriptor by clearing its ownership bit and setting all other bits to 1.

(a) Perfect Filtering (FMB1 = 0, FMB0 = 0)
The DM9102H uses the descriptor buffer as a setup perfect table of 16 destination address. The destination addresses are full 48-bit Ethernet addresses. The DM9102H compares the addresses of any incoming frame to 16 destination addresses of perfect table. The DM9102H will receive incoming frame if address of incoming frame matches one of 16 destination addresses of perfect table. Otherwise, the DM9102H will reject the incoming frame.

(b) Hash Filtering (FMB1 = 0, FMB0 = 1)
The DM9102H uses the descriptor buffer as a setup hash table of 512 bits plus one perfect address. The perfect address is in the low word of the fortieth double-word of Ethernet address table. If the destination address of incoming frame is a multicast address, the DM9102H will use this address to execute CRC (Cyclic Redundancy Check) operation, then CRC operation generates a 48-bit result, DM9102H will take biggest significant nine bits of CRC result to do the index of hash function. If the hash function result is hit (the corresponding bit is 1), the DM9102H will receive the incoming frame. If the hash function result is not hit (the corresponding bit is 0), the DM9102H will reject the incoming frame. However, if the destination address of incoming frame is a physical

address, the DM9102H executes a perfect filtering compared with the perfect address. If the destination address of incoming frame matches perfect address, the DM9102H will receive the incoming frame. Otherwise, the DM9102H will reject the incoming frame.

(c) Inverse Filtering (FMB1 = 1, FMB0 = 0)

The DM9102H compares the addresses of any incoming frame to 16 destination addresses of perfect table. The DM9102H will reject incoming frame if address of incoming frame matches one of 16 destination addresses of perfect table. The DM9102H will receive incoming frame if address of incoming frame done not matches all of 16 destination addresses of perfect table.

(d) Hash-Only Filtering (FMB1 = 1, FMB0 = 1)

The DM9102H uses the descriptor buffer as a setup 512 bits hash table. If DM9102H receives an incoming frame of the destination address is a multicast address or a physical address, the DM9102H will execute a hash function and compare with the hash table. If the hash function result is hit, the DM9102H will receive the incoming frame. Otherwise, the DM9102H will reject the incoming frame.

7.2 Initialization Procedure

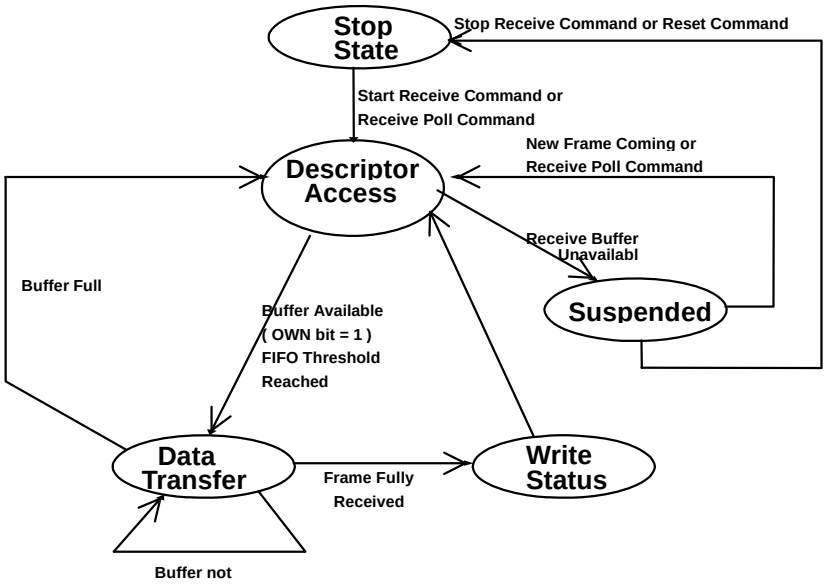
After hardware or software reset, transmit and receive processes are placed in the state of STOP. The DM9102H can accept the host commands to start operation. The general procedure for initialization is described below:
(1) Read/write suitable values for the PCI configuration registers.
(2) Write CR3 and CR4 to provide the starting address of each descriptor list.
(3) Write CR0 to set global host bus operation parameters.
(4) Write CR7 to mask causes of unnecessary interrupt.
(5) Write CR6 to set global parameters and start both receive and transmit processes. Receive and transmit processes will enter the running state and attempt to acquire descriptors from the respective descriptor lists.
(6) Wait for any interrupt.

7.2.1 Data Buffer Processing Algorithm

The data buffer process algorithm is based on the cooperation of the host and the DM9102H. The host sets CR3 (receive descriptor base address) and CR4 (transmit descriptor base address) for the descriptor list initialization. The DM9102H will start the data buffer transfer after the descriptor polling and get the ownership. For detailed processing procedure, please see below.

7.2.2 Receive Data Buffer Processing

Refer to Figure 7-2. The DM9102H always attempts to acquire an extra descriptor in anticipation of the incoming frames. Any incoming frame size covers a few buffer regions and descriptors. The following conditions satisfy the descriptor acquisition attempt:
When start/stop receive sets immediately after being placed in the running state.
When the DM9102H begins writing frame data to a data buffer pointed to by the current descriptor and the buffer ends before the frame ends.
When the DM9102H completes the reception of a frame and the current receiving descriptor is closed.
When receive process is suspended due to no free buffer for the DM9102H and a new frame is received.
When receive polling demand is issued. After acquiring the free descriptor, the DM9102H processes the incoming frame and places it in the acquired descriptor's data buffer. When the whole received frame data has been transferred, the DM9102H will write the status information to the last descriptor. The same process will repeat until it encounters a descriptor flagged as being owned by the host. If this occurs, receive process enters the suspended state and waits the host to service

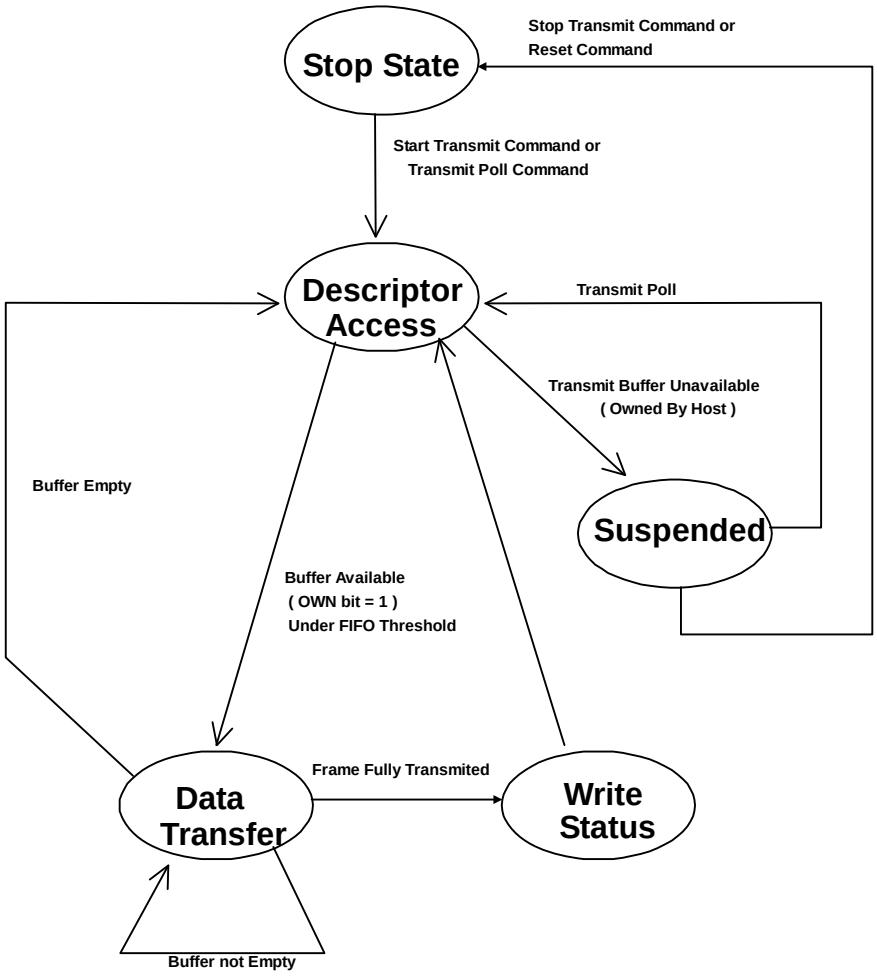


Receive Buffer Management State Transition
Figure 7-2

7.2.3 Transmit Data Buffer Processing

Refer to Figure 7-3. When start/stop transmit command is set and the DM9102H is in running state, transmit process polls transmit descriptor list for frames requiring transmission. When it completes a frame transmission, the status related to the transmitted frame will be written into the transmit descriptor. If the DM9102H detects a descriptor flagged as owned by the host and no transmit buffers are available, transmit process will be suspended. While in the running state, transmit process can simultaneously acquire two frames. As transmit process completes copying the first frame, it immediately polls transmit descriptor list for the second frame. If the second frame is valid, transmit process copies the frame before writing the status information of the first frame.

Both conditions will make transmit process suspend. (i) The DM9102H detects a descriptor owned by the host. (ii) A frame transmission is aborted when a locally induced error is detected. Under either condition, the host driver has to service the condition before the DM9102H can resume.



Transmit Buffer Management State Transition

Figure 7-3

7.3 Network Function

7.3.1 Overview

This chapter will introduce the normal state machine operation and MAC layer management like collision back-off algorithm. In transmit mode, the DM9102H initiates a DMA cycle to access data from a transmit buffer. It prefaces the data with the preamble, the SFD pattern, and it appends a 32-bit CRC. In receive mode, the data is de-serialized by receive mechanism and is fed into the internal FIFO. For detailed process, please see below.

7.3.2 Receive Process and State Machine

a. Reception Initiation
As a preamble being detected on receive data lines, the DM9102H synchronizes itself to the data stream during the preamble and waits for the SFD. The synchronization process is based on byte boundary and the SFD byte is 10101011. If the DM9102H receives a 00 or an 11 after the first 8 preamble bits and before receiving the SFD, the reception process will be terminated.

b. Address Recognition
After initial synchronization, the DM9102H will recognize the 6-byte destination address field. The first bit of the destination address signifies whether it is a physical address (=0) or a multicast address (=1). The DM9102H filters the frame based on the node address of receive address filter setting. If the frame passes the filter, the subsequent serial data will be delivered into the host memory.

c. Frame Decapsulation
The DM9102H checks the CRC bytes of all received frames before releasing the frame along with the CRC to the host processor.

7.3.3 Transmit Process and State Machine

a. Transmission Initiation

Once the host processor prepares a transmit descriptor for the transmit buffer, the host processor signals the DM9102H to take it. After the DM9102H has been notified of this transmit list, the DM9102H will start to move the data bytes from the host memory to the internal transmit FIFO. When the transmit FIFO is adequately filled to the programmed threshold level, or when there is a full frame buffered into the transmit FIFO, the DM9102H begins to encapsulate the frame. The transmit encapsulation is performed by the transmit state machine, which delays the actual transmission onto the network until the network has been idle for a minimum inter frame gap time.

b. Frame Encapsulation
The transmit data frame encapsulation stream consists of two parts: Basic frame beginning and basic frame end. The former contains 56 preamble bits and SFD, the later, FCS. The basic frame read from the host memory includes the destination address, the source address, the type/length field, and the data field. If the data field is less than 46 bytes, the DM9102H will pad the frame with pattern up to 46 bytes.

c. Collision
When concurrent transmissions from two or more nodes occur (termed; collision), the DM9102H halts the transmission of data bytes and begins a jam pattern consisting of AAAAAAAA. At the end of the jam transmission, it begins the back off wait time. If the collision was detected during the preamble transmission, the jam pattern is transmitted after completing the preamble. The back off process is called truncated binary exponential back off. The delay is a random integer multiple of slot times. The number of slot times of delay before the Nth retransmission attempt is chosen as a uniformly distributed random integer in the range:
$0 \le r < 2^k$
k = min (n, N) and N=10

7.3.4 Physical Layer Overview

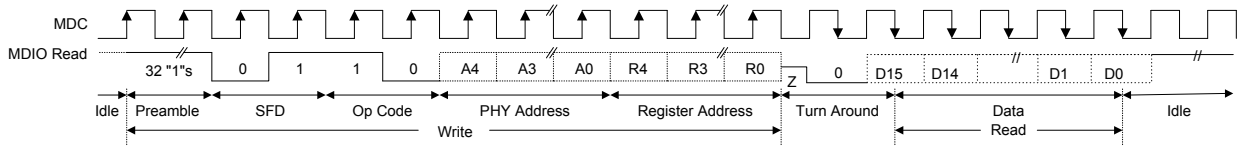
The DM9102H supports 100Mbps and 10Mbps operation. It provides a direct interface either to Unshielded Twisted Pair cable UTP5 for 100BASE-TX fast Ethernet, or UTP5/UTP3 cable for 10BASE-T Ethernet. In physical level operation, it consists of the following functions:

- PCS: 4B5B encode/decode, scramble/de-scramble, and data serialize/parallelize
- NRZ/NRZI, MLT-3 encoder/decoder and driver
- MANCHESTER encoder/decoder
- 10BASE-T filter, driver/receiver, and MANCHESTER encoder/decoder
- Auto. MDI/MDIX detection

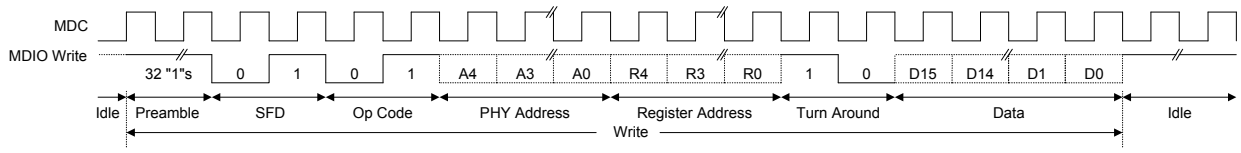
7.4 Serial Management Interface

The serial management interface is used to obtain and control the status of PHY management register set through the internal MDC and MDIO signals, which is control by CR9 bits 19:16. The Management Data Clock (MDC) is equipped with a maximum clock rate of 2.5MHz.
In read/write operation, the management data frame is 64-bit long start with 32 contiguous logic one bits (preamble) synchronization clock cycles on MDC. The Start of Frame Delimiter (SFD) is indicated by a <01> pattern followed by the operation code (OP) :< 10> indicates Read operation and <01> indicates Write operation. Following the OP Code is the 5-bit PHY Address field that is fixed to 00001b. For read operation, a 2-bit turnaround (TA) filing between Register Address field and Data field is provided for MDIO to avoid contention. "Z" stands for the state of high impedance. Following turnaround time, a 16-bit data is read from or written onto management registers.

7.4.1 Management Interface - Read Frame Structure



7.4.2 Management Interface - Write Frame Structure



7.5 Power Management

7.5.1 Overview

The DM9102H supports power management mechanism. It complies with the ACPI Specification Rev 1.0, the Network Device Class Power Management Specification Rev 1.0, and the PCI Bus Power Management Interface Specification Rev 1.0. In addition, it also supports the Wake-On LAN (WOL) which is the feature of the AMD's Magic Packet™ technology. With this function, it cans wakeup a remote sleeping station.

7.5.2 PCI Function Power Management States

The DM9102H supports PCI function power states D0, D3 (hot), D3 (cold), and does not support D1, D2 states. In addition, PCI signals PME# (power management event, open drain) to pin A19 of the standard PCI connector.

D0: normal & fully functional state

D3 (hot): For controller, configuration space, that can be accessed and wake up on LAN circuit, can be enabled. PME# operational circuit is active, full function is supported to detect the wake up Frame & Link status. Because of functions in D3 (hot) must respond to configuration space accesses as long as power and clock are supplied so that they can be returned to D0 state by software.

D3 (cold): If Vcc is removed from a PCI device; all of its PCI functions transition immediately to D3 (cold), no bus transaction is active without pci_clk condition and wake up on LAN operation should be alive. PME# operational circuit is active. Full function is supported under auxiliary power to detect the magic packet & Link status. When power restored, PCI RST# must be asserted and functions will return to D0 with a full PCI Spec. 2.2 compliant power-on reset sequence. The power required in D3 (cold) must be provided by some auxiliary power source.

7.5.3 The Power Management Operation

It complies with the PCI Bus Power Management Interface Specification Rev. 1.0. The Power Management Event (PME#) signal is an optional open drain, active low signal that is intended to be driven low by a PCI function to request a change in its current power management state and/or to indicate that a power management event has occurred.
The PME# signal has been assigned to pin A19 of the standard PCI Connector configuration. The assertion and de-assertion of PME# is asynchronous to the PCI clock.

Software will enable its use by setting the PME_En bit in the PMCSR (write 1 to PMCSR<8>). When a PCI function generates or detects an event that requires the system to change its power state, the function will assert PME#. It must continue to assert PME# until software either clears the PME_En bit (PMCSR<8> is set to 0) or clears the PME_Status bit in the PMCSR (write 1 to PMCSR<15>).

DM9102H supports three main categories of network device wake up events specified in Network Device Class Power Management Rev1.0. That is, the DM9102H can monitor the network for a Link Change, Magic Packet or a Wake-up Frame and notify the system by generating PME# if any of the three events occurs. Programming the PCIUSR (offset = 40h) can select the PME# event, and writing 1 to PMCSR<15> will clear the PME#.

a. Detect Network Link State Change
Any link status change will set the wake up event.

1. Writes 1 into PMCSR<15>(54h) to clear previous PME# status
2. Writes 1 into PMCSR<8> to enable PME# function
3. Writes 1 into PCIUSR<29> to enable the link status change function

b. Active Magic Packet Function
It can be enabled by PCIUSR<27> or optionally enabled by EEPROM setting. The magic node address stored at node address table can use setup frame perfect address filtering mode or loading from EEPROM WORD 10~12 after power on.

1. Writes 1 into PMCSR<15> to clear previous PME status
2. Writes 1 into PMCSR<8> to enable PME# function
3. Writes 1 into PCIUSR<27> to enable magic packet function.

c. Active the Sample Frame Function

It can be enabled by PCIUSR<28>. Sample frame data and corresponding byte mask are loaded into transmit FIFO & receive FIFO before entering D3 (hot). The software driver has to stop the TX/RX process before setting the sample frame and byte mask into the FIFO. Transmit & receive FIFO can be accessed from CR13 & CR14 by programming CR6<28:25> = 0011.

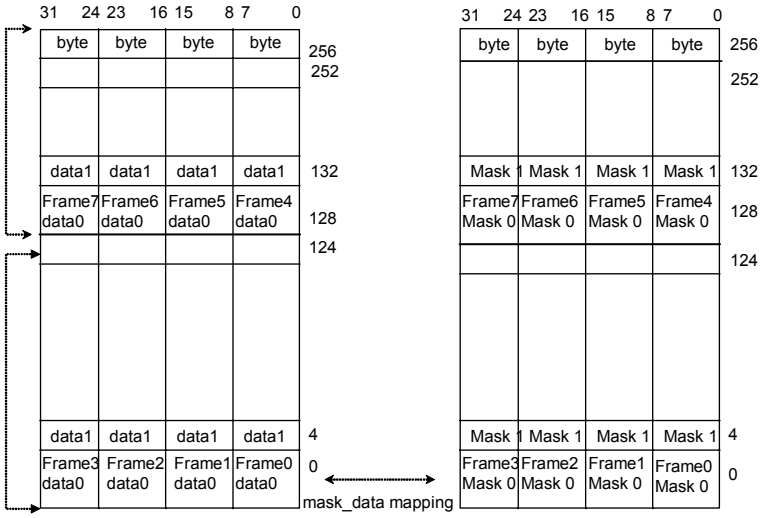
The operational sequence from D0 to D3 should be:
Stop TX/RX process → wait for entering stop state → set test mode, CR6<28:25> = 0011 → programming FIFO contents → exit test mode → enter D3 (hot) state

The sample frame data comparison is completed when the received frame data has exceeded the programmed frame length or when the whole packet has been fully received. The operation procedure is shown below.

DM9102A can handle 8 sample frames. The max byte count is 128 byte each sample frame.

bit1	bit0	description
0	0	this byte don't care
0	1	this byte musk check
1	0	this byte don't care
1	1	end of mask(sample frame)

Frame mask definition: only used bit0&bit1 per byte



CR13: Sample Frame Access Register

Name	General definition	Bit8:3	Type
TxFIFO	Transmit FIFO access port	32h	R/W
RxFIFO	Receive FIFO access port	35h	RW
DiagReset	General reset for diagnostic pointer port	38h	RW

In DiagReset port there are 7 bits:

Bit 0: Clear TX FIFO write_ address to 0
Bit 1: Clear TX FIFO read_ address to 0
Bit 2: Clear RX FIFO write_ address to 0
Bit 3: Clear RX FIFO read_ address to 0
Bit 4: Reserved
Bit 5: Set TX FIFO write_ address to 080H
Bit 6: Set RX FIFO write_ address to 080H

7.6 Sample Frame Programming Guide:

1. Enter the sample frame access mode:
   Set CR6<28:25>=0011

2. Reset the TX/RX FIFO, write pointer to offset 0:
   Write 38H to CR13<8:3>
   Write 01h to CR14 (reset)
   Write 00h to CR14 (clear)

3. Write the sample frame 0-3 data to RX FIFO:
   Write 35H to CR13<8:3>
   Write xxxxxxxxh to CR14 (Frame1~3 first byte)
   Write xxxxxxxxh to CR14 (Frame1~3 second byte)
   :
   :
   Repeat write until all frame data written to RX FIFO

4. Reset RX FIFO, write pointer to offset 080H:
   Write 38H to CR13<8:3>
   Write 40H to CR14 (reset)
   Write 00H to CR14 (clear)

5. Write the sample frame 4-7 to RX FIFO:
   Write 35H to CR13<8:3>
   Write xxxxxxxxh to CR14 (Frame4~7 first byte)
   Write xxxxxxxxh to CR14 (Frame4~7 second byte)
   :
   :
   Repeat write until all frame data written to RX FIFO

6. Write the sample frame 0-3 mask to TX FIFO:
   Write 32H to CR13<8:3>
   Write xxxxxxxxh to CR14 (Frame0~3 first mask byte)
   Write xxxxxxxxh to CR14 (Frame0~3 second mask byte)
   :
   :
   Repeat write until all frame mask which is written to TX FIFO

7. Reset TX FIFO, write pointer to offset 080H:
   Write 38H to CR13<8:3>
   Write 20H to CR14 (reset)
   Write 00H to CR14 (clear)

8. Write the sample frame 4-7 mask to TX FIFO:
   Write 32H to CR13<8:3>
   Write xxxxxxxxh to CR14 (Frame4~7 first mask byte)
   Write xxxxxxxxh to CR14 (Frame4~7 second mask byte)
   :
   :
   Repeat write until all frame masks is written to TX FIFO

7.7 EEPROM Overview

The first 13 words of Configuration EEPROM are loaded into the DM9102H after power-on-reset for the settings of the power management, system ID and Ethernet address. The format of the EEPROM is as followed

The format of EEPROM

Field Name	Word Offset	Word Size
Subsystem Vendor ID	0	1
Subsystem ID	1	1
Reserved	2	2
NCE and Auto_ load_ control	4	1
PCI Vendor ID	5	1
PCI Device ID	6	1
PMCSR and PMC	7	1
Reserved	8	2
Ethernet Address	10	3

If bit6=1, WOL is LEVEL signal.

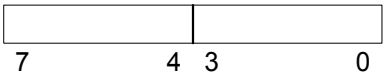
7.7.1 Subsystem ID Block

Every card has a Subsystem ID to indicate the information of system vendor. The content will be transferred into the PCI configuration space 2CH.

7.7.2Vendor ID

Vendor ID & Device ID can be set in EEPROM content & auto-loaded to PCI configuration register after reset. (Default value = 1282H, 9102H) This function must be selectable for enable by Auto_ Load_ Control (word offset 04 bit [3:0] of EEPROM).

7.7.3 Word Offset (04): Auto_ Load_ Control

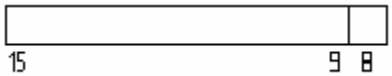


Bit3~0: “1010” to enable auto-load of PCI Vendor_ ID & Device_ ID.

Bit7~4: “1X1X” to enable auto-load of NCE, PME & PMC & PMCSR to PCI configuration space. Bit 4 and 6 are used to control the polarity and pulse mode of the WOL pin.

If bit4 = 0, WOL is Active HIGH.
If bit4=1, WOL is Active LOW
If bit6 = 0, WOL is PULSE signal

7.7.4 Word Offset (04): New_ Capabilities_ Enable

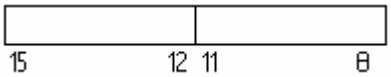


Bit0: Directly mapping to bit20 (New Capabilities) of the PCICS
If Bit9=1, Bit [12:10] mapping to bit [18:16] of the PCIPMR and Bit [15:13] mapping to bit [24:22] of the PCIPMR.

7.7.5 Word Offset (07): PMC

Bit7~3: Directly mapping to bit [31:27] of the PCIPMR.
Bit2~0: Directly mapping to bit [21, 26:25] of the PCIPMR.

7.7.6 Word Offset (07): Control



Bit 15: Reserved
Bit 14: Disable to power-down PHY if ISOLATE pin is low.
Bit 13: Clear PMCSR [1:0] if RST# pin is low
Bit 12: PME# is not pulse mode

Bit 11: Set to disable the output of WOL pin.
Bit 10: Set to disable the output of PME# pin.
Bit 9: Set to enable the link change wake up event.
Bit 8: Set to enable the Magic packet wake up event.

7.7.7 Word Offset (10~12): Ethernet Address

Address 0 = EEPROM Word 10 low byte
Address 1 = EEPROM Word 10 high byte
Address 2 = EEPROM Word 11 low byte
Address 3 = EEPROM Word 11 high byte
Address 4 = EEPROM Word 12 low byte
Address 5 = EEPROM Word 12 high byte

7.7.8 Example of DM9102H EEPROM Format

Total Size: 128 Bytes

Field Name	Offset (Byte)	Size (Bytes)	Value (Hex)	Commentary
Sub-Vendor ID	0	2	1282H	ID Block
Sub-Device ID	2	2	9102H	
Reserved1	4	4	00000000	
Auto_Load_Control	8	1	00	Auto-load function definition: Bit 3~0 = 1010 → Auto-Load PCI Vendor ID/Device ID enabled Bit 7~4 = 1x1x → Auto-Load NCE, PMC/PMCSR enabled
New_Capabilities_Enable (NCE)	9	1	00	Please refer to DM9102H Spec.
PCI Vendor ID	10	2	1282H	If Auto-Load PCI Vendor ID/Device ID function disabled, the PCI Vendor ID/Device ID will use the default values (1282H, 9102H).
PCI Device ID	12	2	9102H	
Power Management Capabilities (PMC)	14	1	00	Please refer to DM9102H Spec.
Power Management Control/Status (PMCSR)	15	1	00	Please refer to DM9102H Spec.
Reserved2	16	4	00	
IEEE Network Address	20	6	-	Controller Info Header
Driver area	26	102	-	For software driver

7.8 External MII Interface

DM9102H provides one external MII interface sharing with all the pins with Boot ROM interface. This external MII interface can be connected with external PHYceiver such as Home Networking PHYceiver or other future technology applications. This external MII interface can be set up by hardware and software. The setup methods are listed as below:

	Test 1 (pin 37)	Test 2 (pin 71)	Clkrun# (pin 36)	EECK (pin 79)	EEDO (pin 78)	
Normal Operation	0	1	X	X	X	
External MII mode	0	0	0	0	1/0	**Note 1**
Internal Test mode	1	X	X	X	X	

Note 1: External MII mode
EEDO = 1(pulled high): only external PHY is selected.
EEDO = 0(floating) & MII_ Mode = 1: Select external PHY
EEDO = 0(floating) & MII_ Mode = 0: Select internal PHY
Where MII_ Mode is the bit 18 of CR6.

7.8.1 The Sharing Pin Table

(o): output, (i): input, (b): bi-direction

	Normal Operation	External MII Interface
	Boot ROM interface	External MII interface
		TEST2= 0
Pin		
62	MD0/EEDI	MII_MDIO/EEDI(b)
63	MD1	MII_RXD2 (i)
64	MD2	MII_RXD1 (i)
65	MD3	MII_RXD0 (i)
66	MD4	MII_RXDV (i)
67	MD5	MII_RXER (i)
68	MD6	MII_CRS (i)
69	MD7	MII_RXCLK (i)
77	NC	MII_COL(i)
78	EEDO	MII_TXD0/EEDO(o)
79	EECK	MII_TXD1/EECK (o)
83	GNT2#	MII_TXEN(o)
84	REQ2#	MII_TXCLK (i)
87	TRF_LED	MII_TXD2(o)
88	FDX_LED	MII_TXD3(o)
89	SPD100_LED	MII_MDC(o)
90	SPD10_LED	MII_RXD3(i)

Where NC is no connection

8. DC and AC Electrical Characteristics

8.1 Absolute Maximum Ratings (TA, Min.=0°C, Max.=+70°C)

Symbol	Parameter	Min.	Max.	Unit	Conditions
DVDD	Supply Voltage	-0.3	3.6	V	
DVDD18,AVDD18	Supply Voltage	-0.3	1.85	V	
VIN	DC Input Voltage (VIN)	-0.5	5.5	V	
VOUT	DC Output Voltage (VOUT)	-0.3	3.6	V	
Tstg	Storage Temperature Rang (Tstg)	-65	+150	°C	
LT	Lead Temp. (TL, Soldering, 10 sec.)	—	+260	°C	DM9102HEP

8.2 Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
DVDD,AVDD	Supply Voltage	3.135	3.300	3.465	V	
DVDD18,AVDD18	Supply Voltage	1.71	1.80	1.89	V	
PD (Power Dissipation)	100BASE-TX	---	130	---	mA	3.3V
	10BASE-T TX	---	170	---	mA	3.3V
	10BASE-T TX (100% utilization)	---	160	---	mA	3.3V,power saving
	10BASE-T idle	---	60	---	mA	3.3V,power saving
	Auto-negotiation	---	60	---	mA	3.3V
	Power Down Mode	---	20	---	mA	3.3V
	Power Down Mode (system clock off)	---	6	---	mA	3.3V

Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

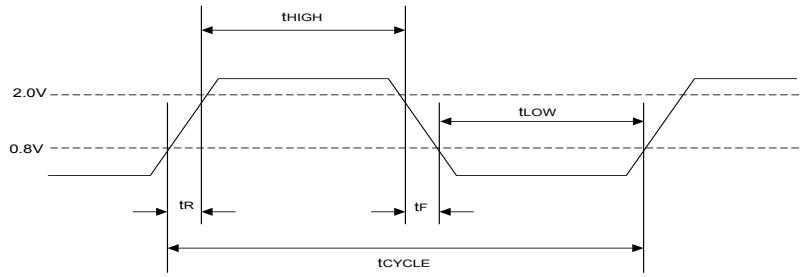
8.3 DC Electrical Characteristics

(3.135V<AV_{DD}, DV_{DD}<3.465V, unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Inputs						
V_{IL}	Input Low Voltage	-	-	0.8	V	
V_{IH}	Input High Voltage	2.0	-	-	V	
I_{IL}	Input Low Leakage Current	-	-	1	uA	V_{IN} = 0V
I_{IH}	Input High Leakage Current	-1	-	-	uA	V_{IN} = 3.3V
Outputs						
V_{OL}	Output Low Voltage	-	-	0.4	V	I_{OL} = 4mA
V_{OH}	Output High Voltage	2.4	-	-	V	I_{OH} = -4mA
Receiver						
V_{ICM}	RX+/RX- Common mode Input Voltage	-	1.8	-	V	100 Ω Termination Across
Transmitter						
V_{TD100}	100TX+/- Differential Output Voltage	1.9	2.0	2.1	V	Peak to Peak
V_{TD10}	10TX+/- Differential Output Voltage	4.4	5	5.6	V	Peak to Peak
I_{TD100}	100TX+/- Differential Output Current	19	20	21	mA	Absolute Value
I_{TD10}	10TX+/- Differential Output Current	44	50	56	mA	Absolute Value

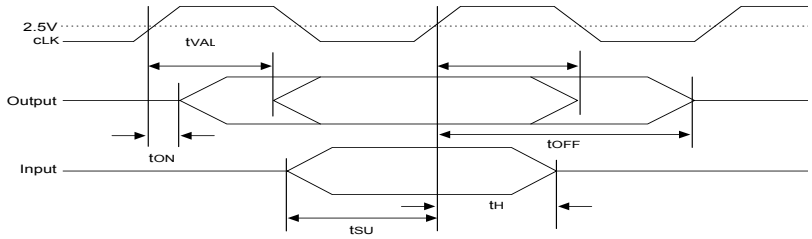
8.4 AC Electrical Characteristics & Timing Waveforms

8.4.1 PCI Clock Specifications Timing



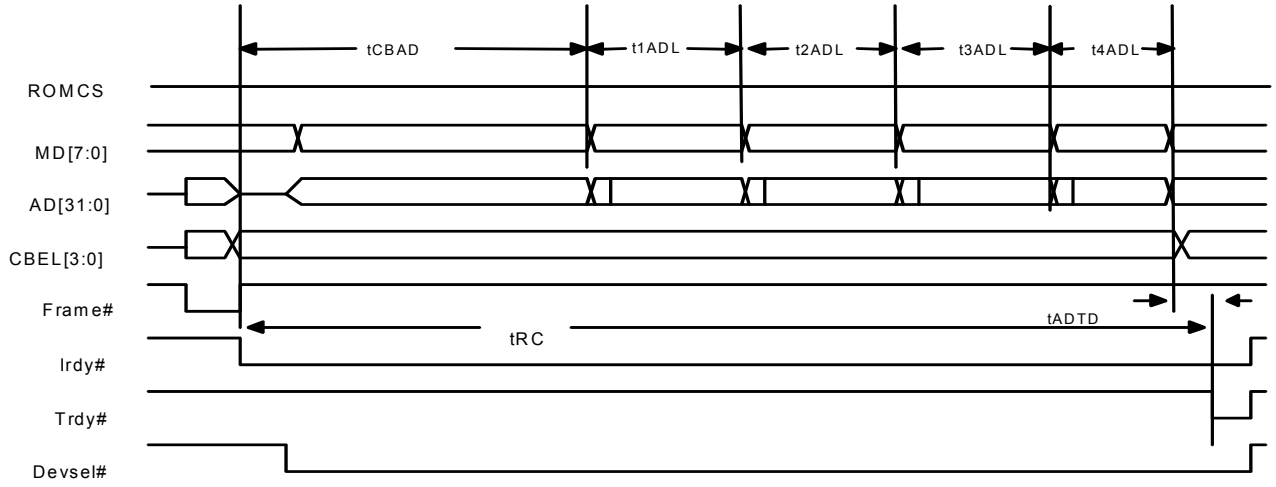
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_R	PCI_CLK Rising Time	-	-	4	ns	-
t_F	PCI_CLK Falling Time	-	-	4	ns	-
t_{CYCLE}	Cycle Time	25	30	-	ns	-
t_{HIGH}	PCI_CLK High Time	12	-	-	ns	-
t_{LOW}	PCI_CLK Low Time	12	-	-	ns	-

8.4.2 Other PCI Signals Timing Diagram



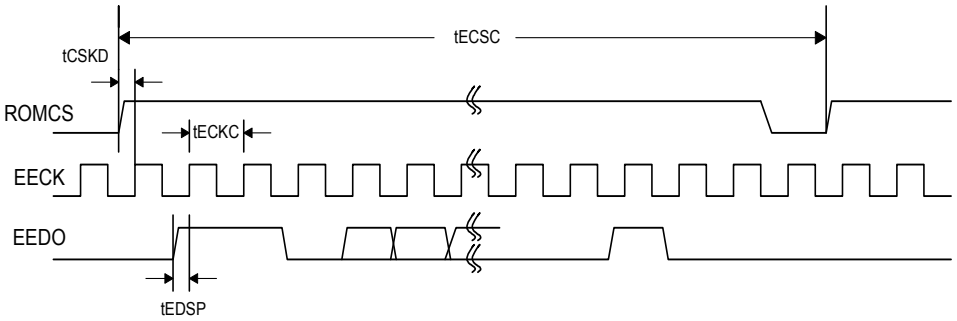
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{VAL}	Clk-To-Signal Valid Delay	2	-	13	ns	Cload = 50 pF
t_{ON}	Float-To-Active Delay From Clk	2	-	-	ns	-
t_{OFF}	Active-To-Float Delay From Clk	-	-	28	ns	-
t_{SU}	Input Signal Valid Setup Time Before Clk	7	-	-	ns	-
t_H	Input Signal Hold Time From Clk	0	-	-	ns	-

8.4.3 Boot ROM Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tRC	Read Cycle Time	-	50	-	PCI clock	-
tCBAD	Bus Command to First Address Delay	-	18	-	PCI clock	-
T1ADL	First Address Length	-	8	-	PCI clock	-
T2ADL	Second Address Length	-	8	-	PCI clock	-
T3ADL	Third Address Length	-	8	-	PCI clock	-
T4ADL	Fourth Address Length	-	7	-	PCI clock	-
tADTD	End of Address to Trdy Active	-	1	-	PCI clock	-

8.4.4 EEPROM Read Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tECKC	Serial ROM Clock EECK Period	-	2560	-	ns	-
tECSC	Read Cycle Time	-	71680	-	ns	-
tCSKD	Delay from ROMCS High to EECK High	-	1600	-	ns	-
tEDSP	Setup Time of EEDO to EECK	-	960	-	ns	-

8.4.5 TP Interface

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
$t_{TR/F}$	100TX+/- Differential Rise/Fall Time	3.0	-	5.0	ns	
t_{TM}	100TX+/- Differential Rise/Fall Time Mismatch	0	-	0.5	ns	
t_{TDC}	100TX+/- Differential Output Duty Cycle Distortion	0	-	0.5	ns	
$t_{T/T}$	100TX+/- Differential Output Peak-to-Peak Jitter	0	-	1.4	ns	
X_{OST}	100TX+/- Differential Voltage Overshoot	0	-	5	%	

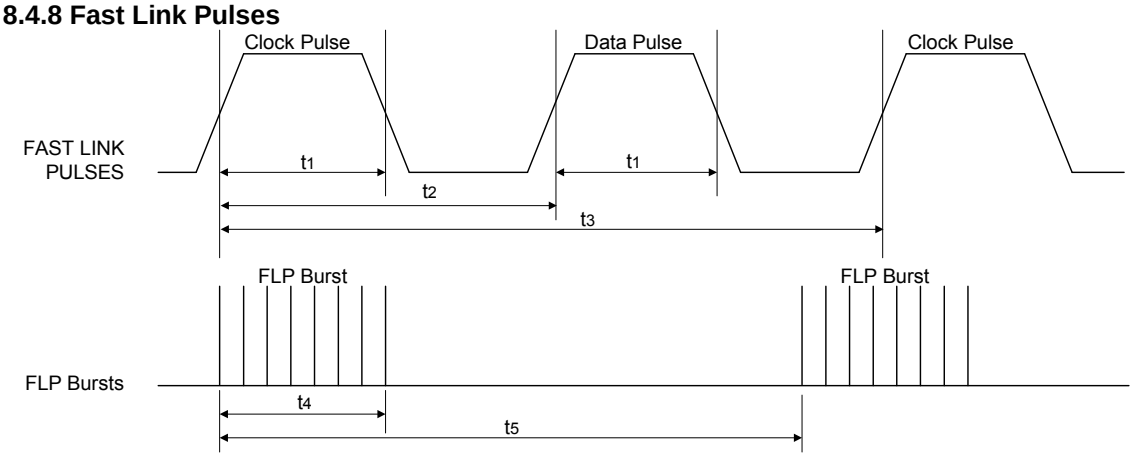
8.4.6 Oscillator/Crystal Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{CKC}	OSC Cycle Time	39.998	40	40.002	ns	+/-50ppm
T_{PWH}	OSC Pulse Width High	16	20	24	ns	
T_{PWL}	OSC Pulse Width Low	16	20	24	ns	

8.4.7 Auto-negotiation and Fast Link Pulse Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_1	Clock/Data Pulse Width	-	100	-	ns	
t_2	Clock Pulse To Data Pulse Period	55.5	62.5	69.5	us	DATA = 1
t_3	Clock Pulse To Clock Pulse Period	111	125	139	us	
t_4	FLP Burst Width	-	2	-	ms	
t_5	FLP Burst To FLP Burst Period	8	16	24	ms	
-	Clock/Data Pulses in a Burst	17		33	#	

8.4.8 Fast Link Pulses



9. Application Notes

9.1 Network Interface Signal Routing

Place the transformer as close as possible to the RJ-45 connector. Place all the 50Ω resistors as close as possible to the DM9102H RX± and TX± pins. Traces routed from RX± and TX± to the transformer should run in close pairs directly to the transformer. The designer should be careful not to cross the transmit and receive pairs. As always, vias should be avoided as much as possible. The network interface should be void of any signals other than the TX± and RX± pairs between the RJ-45 to the transformer and the transformer to the DM9102H. There should be no power or ground planes in the area under the network side of the transformer to include the area under the RJ-45 connector (Refer to Figure 9-4-1 and 9-5). Keep chassis ground away from all active signals. The RJ-45 connector and any unused pins should be tied to chassis ground through a resistor divider network and a 2KV bypass capacitor.

The Band Gap resistor should be placed as physically close to pin 101 and 102 as possible (refer to Figure 9-1 and 9-2). The designer should not run any high-speed signal near the Band Gap resistor placement.

9.2 10Base-T/100Base-TX Application

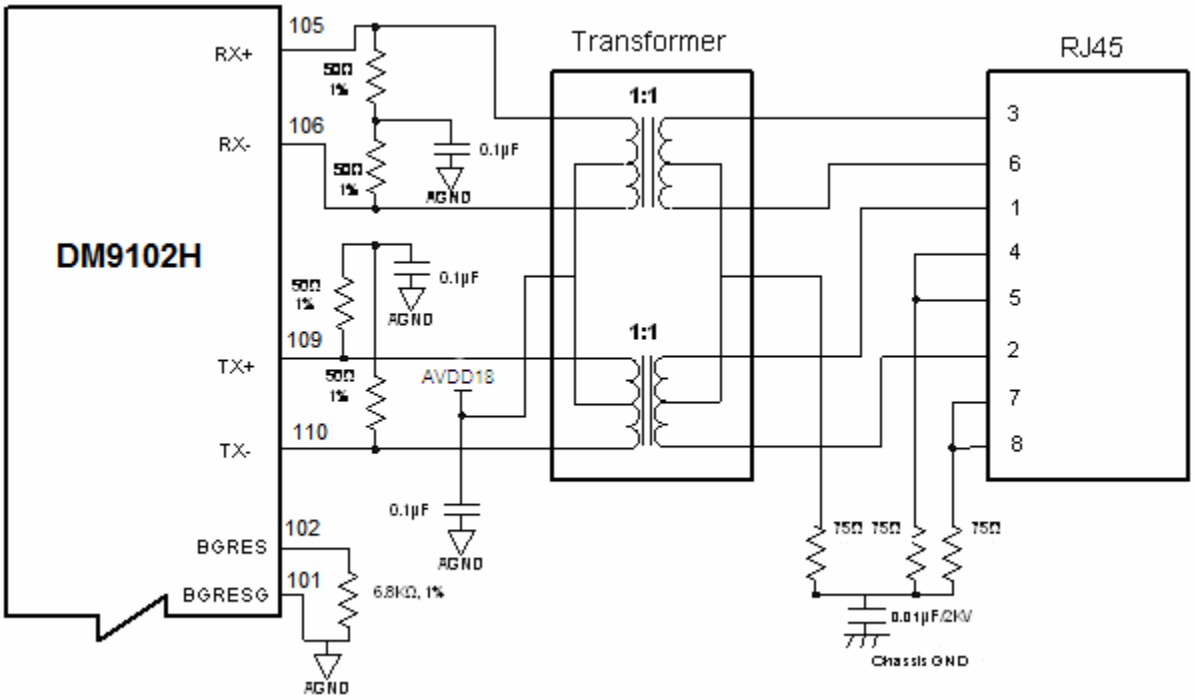


Figure 9-1

9.3 10Base-T/100Base-TX (Power Reduction and non-auto-MDIX Application)

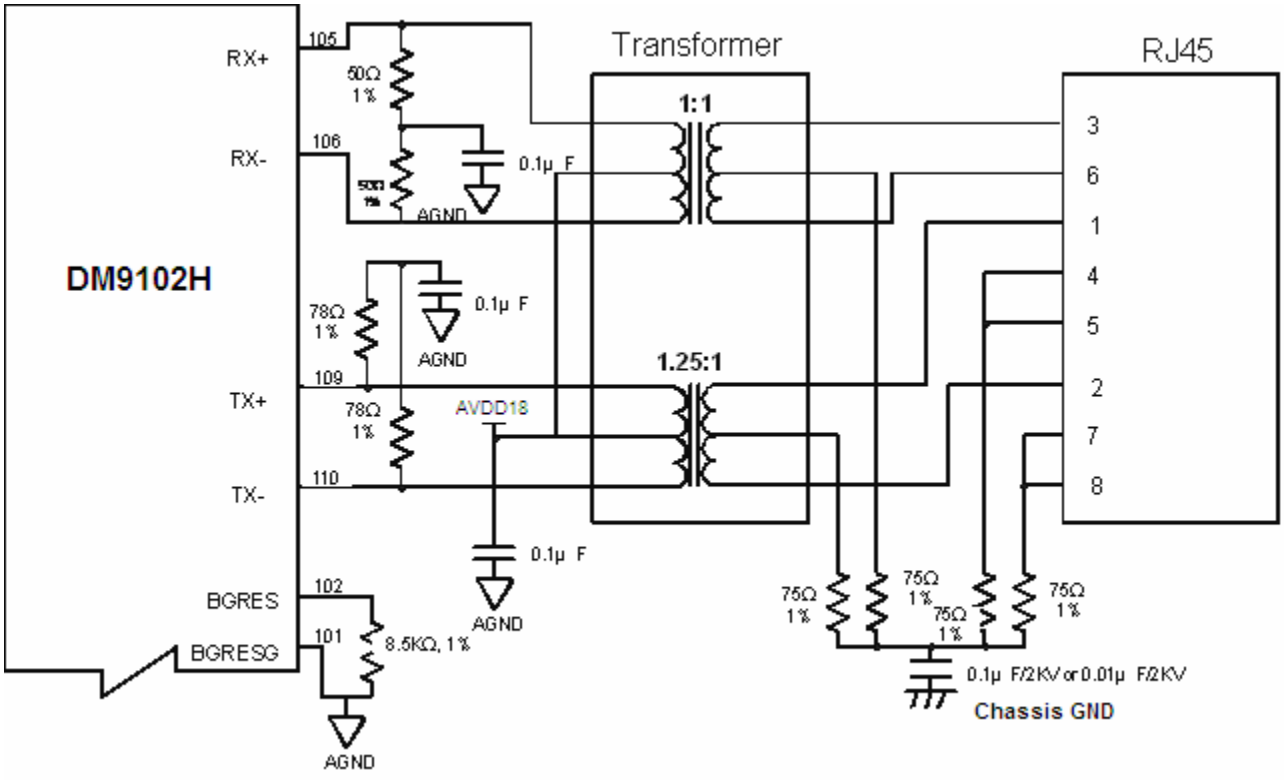


Figure 9-2

9.4 Power Supply Decoupling Capacitors

- Place all the decoupling capacitors for all the power supply pins as close as possible to the power pads of the DM9102H (no more than 2.5mm from the pins mentioned above.) The recommended decoupling capacitor is 0.1μF or 0.01μF.
- The decoupling of PCB layout and power supply should provide sufficient decoupling to achieve the following when measured at the device:
  (1) All DVDDs and AVDDs should be within 50m Vpp of each other,
  (2) All DGNDs and AGNDs should be within 50m Vpp of each other.
  (3) The resultant AC noise voltage measured across each DVDD/DGND set and AVDD/AGND set should be less than 100m Vpp.
- The 0.1-0.01μF decoupling capacitor should be connected between each DVDD/DGND set and AVDD/AGND set be placed as close as possible to the pins of DM9102H. The conservative approach is to use two decoupling capacitors on each DVDD/DGND set and AVDD/AGND set. The 0.1μF capacitor is used for low frequency noise and the 0.01μF one is for high frequency noise on the power supply.
- The AVDD connection to the transmit center tap of the magnetic has to be well decoupled to minimize common mode noise injection from the power supply into the twisted pair cable. It is recommended that a 0.01 μF decoupling capacitor should be placed between the centers tap AVDD to AGND ground plane. This decoupling capacitor should be placed as close as possible to the center tap of the magnetic.

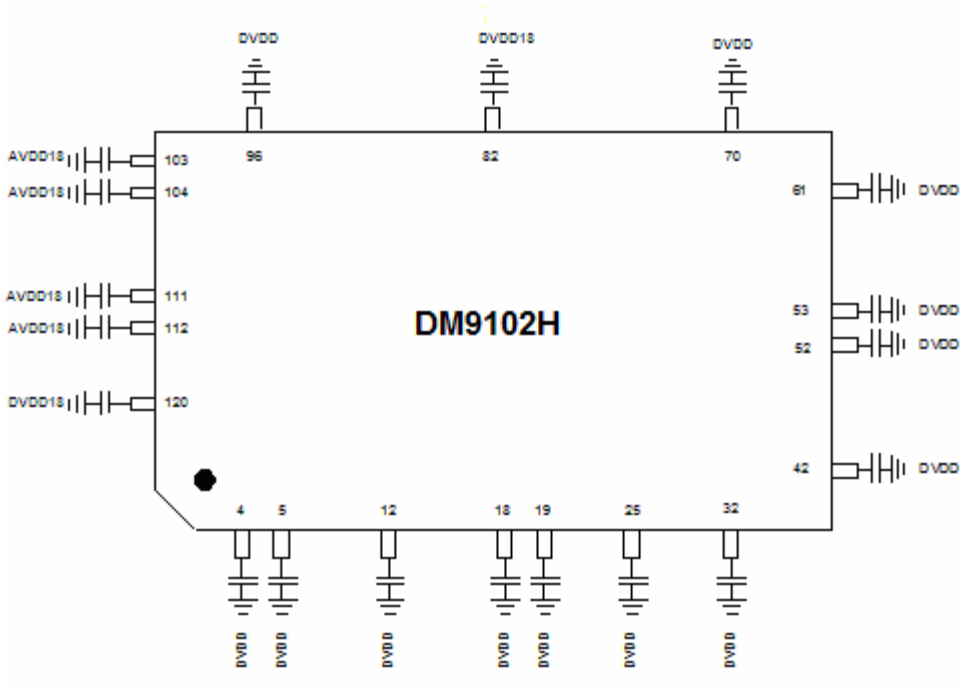


Figure 9-3

9.5 Ground Plane Layout

- Place a single ground plane approach to minimize EMI. Bad ground plane partitioning can cause more EMI emissions that could make the network interface card (NIC) not compliant with specific FCC part 15 and CE regulations.
- The ground plane must be separated into Analog ground domain and Digital ground domain. The line which connects the analog ground domain and digital ground domain should be far away from the AGND pins of DM9102H (see Figure 9-4-1).
- All AGND pins (pin 100, 107, 108) could not directly short each other (see Figure 9-4-3). It must be directly connected to the analog ground domain (see Figure 9-4-2).
- The analog ground domain area is as large as possible

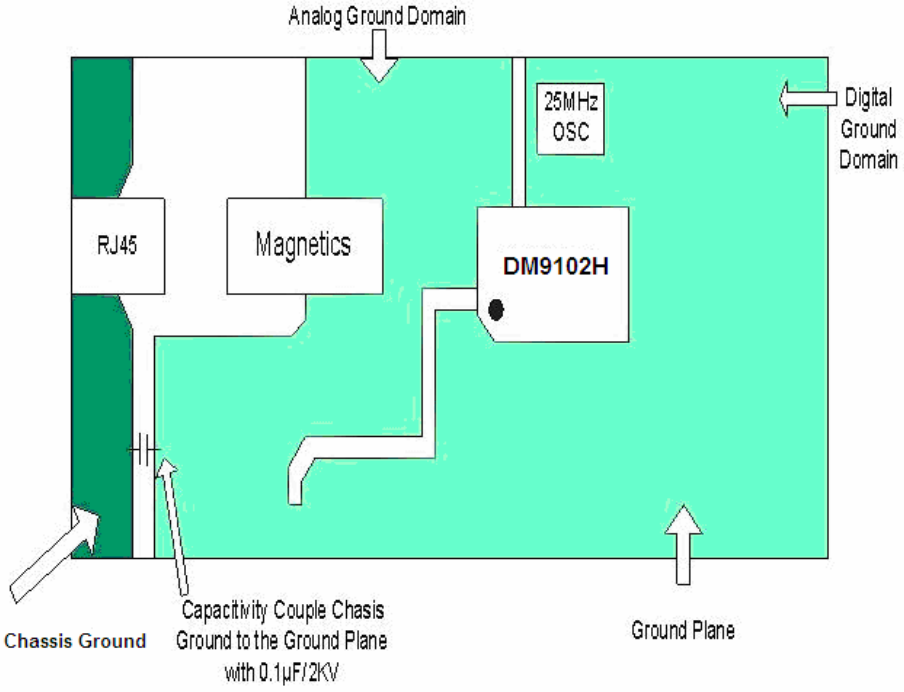


Figure 9-4-1

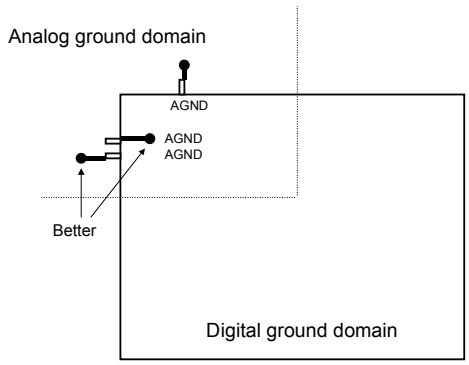


Figure 9-4-2

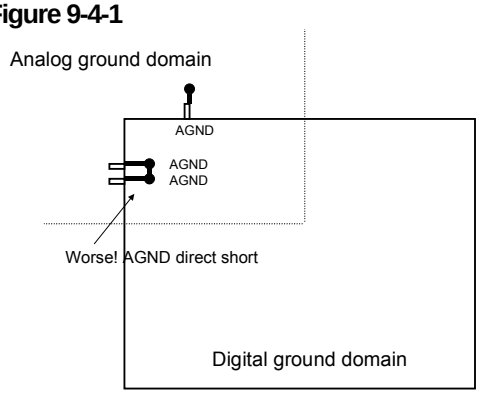


Figure 9-4-3

9.6 Power Plane Partitioning

- The power planes are approximately illustrated in Figure 9-4. The ferrite bead used should have impedance 100Ω at 100MHz and 250mA above. A suitable bead is the Panasonic surface mound bead, part number EXCCL4532U or an equivalent. 10μF, 0.1μF and 0.01μF electrolytic bypass capacitors should be connected between VDD and GND at each side of the ferrite bead.
- Separate analog power planes from noisy logic power planes.

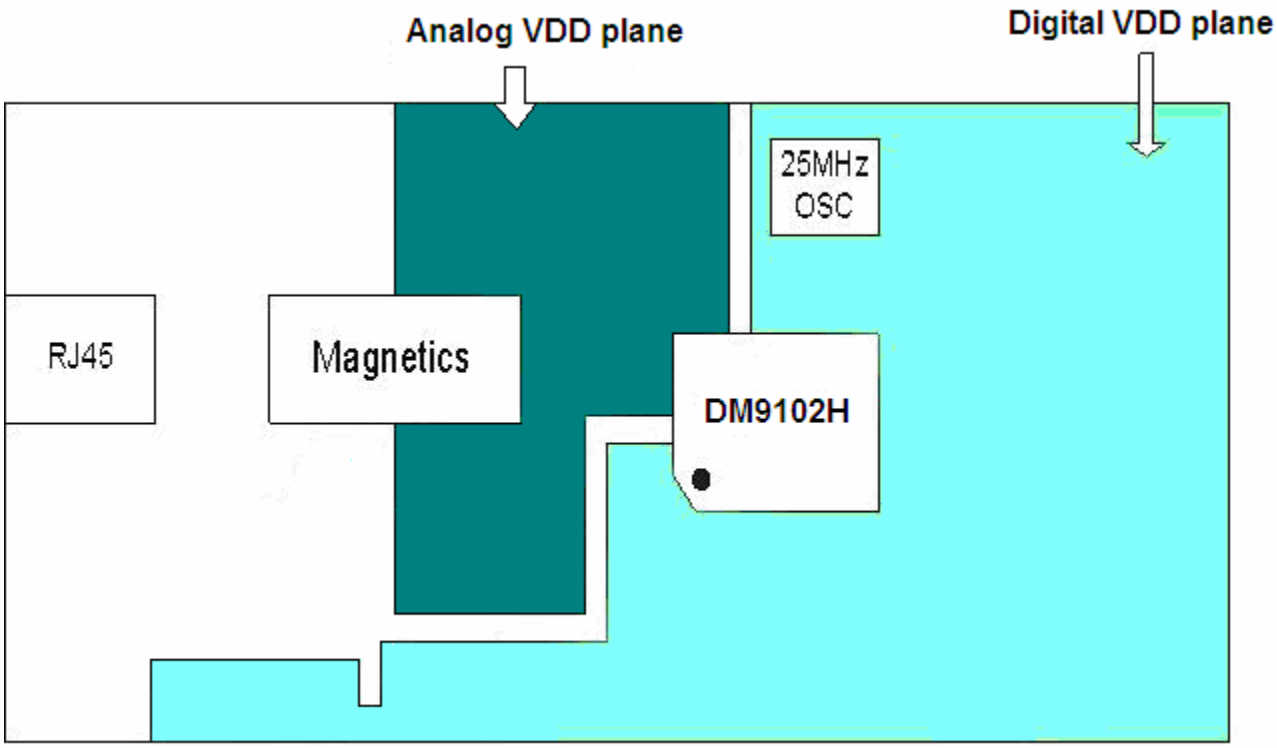


Figure 9-5

9.7 Magnetics Selection Guide

Refer to the following tables 9-1 and 9-2 for 10/100M magnetic sources and specification requirements. The magnetics which meets these requirements are available from a variety of magnetic manufacturers. Designers should test and qualify all magnetic specifications before using them in an application. The magnetics listed in the following tables are electrical equivalents, but may not be pin-to-pin equivalents. Designers should test and qualify all magnetic specifications before using them in an application. RoHS regulations, please contact with your magnetic vendor, this table only for you reference

Manufacturer	Part Number
Pulse Engineering	PE-68515, H1102
YCL	PH163112, PH163539
DELTA	LFE8505-DC , LFE8563-DC, LFE8583-DC
GTS	FC-618SM
MACOM	HS9016, HS9024

•

Table 9-1: 10/100M Magnetic Sources

Parameter	Values	Units	Test Condition
Tx / RX turns ratio	1:1 CT / 1:1	-	-
Inductance	350	μH (Min)	-
Insertion loss	1.1	dB (Max)	1 – 100 MHz
Return loss	-18	dB (Min)	1 –30 MHz
	-14	dB (Min)	30 – 60 MHz
	-12	dB (Min)	60 – 80 MHz
Differential to common mode rejection	-40	dB (Min)	1 – 60 MHz
	-30	dB (Min)	60 – 100 MHz
Transformer isolation	1500	V	-

Table 9-2: Magnetic Specification Requirements

9.8 Crystal Selection Guide

- A crystal can be used to generate the 25MHz reference clock instead of an oscillator. The crystal must be a fundamental type, series-resonant, connected to X1 and X2, and shunt to ground with 22pF capacitors. (See Table 9-3 and Figure 9-6.)

PARAMETER	SPEC
Type	Fundamental, series-resonant
Frequency	25 MHz +/-0.003%
Equivalent Series Resistance	25 ohms max
Load Capacitance	22 pF typ.
Case Capacitance	7 pF max.
Power Dissipation	1mW max.

Table 9-3: Crystal Specifications

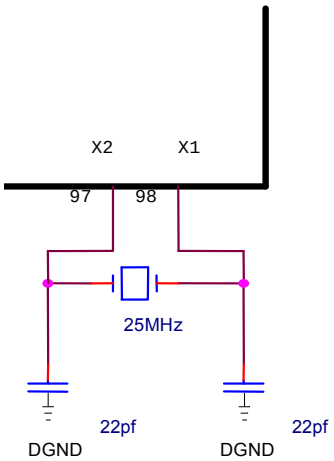
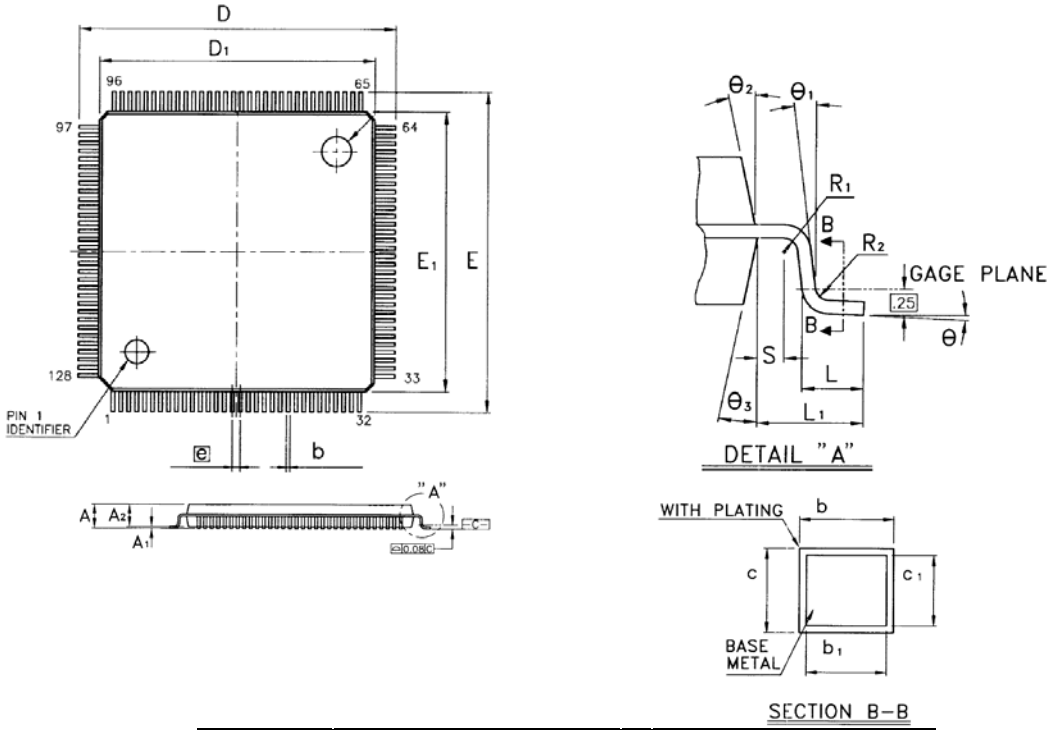


Figure 9-6
Crystal Circuit Diagram

10. Package Information

128 Pins LQFP Package Outline Information:



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.60	-	-	0.063
A_1	0.05	-	-	0.002	-	-
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b_1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	-	0.20	0.004	-	0.008
c_1	0.09	-	0.16	0.004	-	0.006
D	15.85	16.00	16.15	0.624	0.630	0.636
D_1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E_1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	-	-	0.003	-	-
R_2	0.08	-	0.20	0.003	-	0.008
S	0.20	-	-	0.008	-	-
θ	0°	3.5^o	7°	0°	3.5^o	7°
θ_1	0°	-	-	0°	-	-
θ_2	12° TYP			12° TYP		
θ_3	12° TYP			12° TYP		

1. Dimension D_1 and E_1 do not include resin fin.
2. All dimensions are base on metric system.
3. General appearance spec should base on its final visual inspection spec.

11. Ordering Information

Part Number	Pin Count	Package
DM9102HEP	128	LQFP(Pb-Free)

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