



DM9008CEP Product Brief

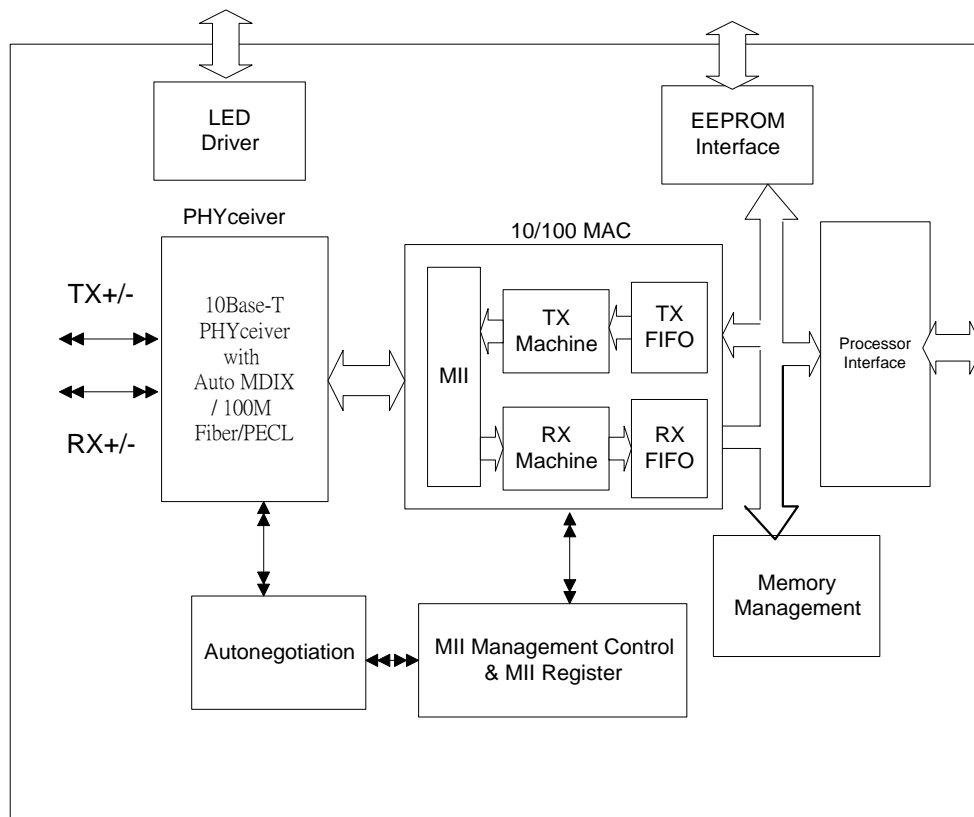
Ethernet Controller with General Processor Interface

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The DM9008C is a fully integrated and cost-effective low pin count Ethernet controller with a general processor interface, a Medial Access Control (MAC), a 10Base-T PHY and 16K Byte SRAM. It is designed with low power and high performance process that support 3.3V with 5V IO tolerance.

The DM9008C supports 8-bit and 16-bit data interfaces to internal memory accesses for various processors. The PHY of the DM9008C can interface to the UTP3, 4, 5 in 10Base-T with HP Auto-MDIX. It is fully compliant with the IEEE 802.3 Spec. Its auto-negotiation function will automatically configure the DM9008C to take the maximum advantage of its abilities. The DM9008C also supports IEEE 802.3x full-duplex flow control...

Block Diagram



Specifications

- Supports processor interface: byte/word of I/O command to internal memory data operation
- Integrated 10M transceiver With HP Auto-MDIX
- Supports back pressure mode for half-duplex
- IEEE802.3x flow control for full-duplex mode
- Supports wakeup frame, link status change and magic packet events for remote wake up
- Support 100M Fiber interface.
- Integrated 16K Byte SRAM
- Build in 3.3V to 1.8V regulator
- Supports IP/TCP/UDP checksum generation and checking
- Supports early Transmit
- Supports automatically load vendor ID and product ID from EEPROM
- Optional EEPROM configuration
- Very low power consumption mode:
 - Power reduced mode (cable detection)
 - Power down mode
 - Selectable TX drivers for 1:1 or 1.25:1 transformers for additional power reduction.
- Compatible with 3.3V and 5.0V tolerant I/O
- DSP architecture PHY Transceiver.
- 48-pin LQFP, 0.18 um process

Application

VoIP CPE (ATA, IP Phone, Video Phone)

IP STB, IPC, Internet Radio

Ordering Information

Part Number	Pin Count	Package
DM9008CEP	48	LQFP (Pb-Free)

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