

# DAVICOM Semiconductor, Inc.

**DM5866**

960H and 720H 4 channels NTSC/PAL  
Decoder

**DATA SHEET**

*Final*

*Version: DM5866-DS-F01  
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## REVISION HISTORY:

Date	Revision	Description
2012/02/02	1.1	Initial release
2012/02/04	1.2	Application schematics modified

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## Introduction

The DM5866 is a high-end 4-channel video decoder designed for cameras with Sony's new 960H CCD sensor. The DM5866 converts 4 channels of 9/6.5 MHz analog CVBS signals to 4 channels of digital 36/27 MHz CCIR656 signals. The DM5866 integrates two internal PLLs, and decodes both 960H and 720H videos using the same (27MHz) external clock source. The DM5866 also features a patented fast switch function. With the fast switch function, the DM5866 can decode up to 8 analog CVBS with little frame rate loss.

The DM5866 also includes five audio ADCs and one audio DAC. Audio cascade up to 16 channels is also supported.

## Features

### Video Decoder

- Accepts NTSC (M,J), PAL (B, D, G, H, I, M, Nc) and SONY 960H CCD Camera
- Each 2 of the 4 video decoders could be programmed to operate at 27 or 36MHz.
- Hardware Fast Switch function
- Fast Switch also controllable by software or external pin
- Software channel ID in active region
- Four 10-bits video ADCs with built in 9/6.5 MHz analog low pass filter
- Automatic gain control for Luminance and Chrominance
- Programmable brightness, contrast, saturation, hue, and sharpness
- 5-H comb filter for YC separation
- Chrominance line filter for PAL phase error
- DLL for video synchronization, supports 27MHz crystal within +/-1000 ppm variance
- Advanced video synchronization for weak and noisy CVBS. Supports video signal transmitted by 500-meter long cable
- Up to 5 CCIR656 output interfaces which could be configured as 5 sets of CCIR656 (36/27MHz) or 3 sets of TDM2 (72/54MHz) or 3 set of TDM4 (144/108MHz)
- Support line lock camera

### Audio Codecs

- Five audio ADCs and one audio DAC are integrated
- Master I2S/DSP playback, record and audio-mixing
- Supports extended I2S/DSP format transmitting up to 16 audio channels using one data pin
- Audio cascade up to 16 channels
- 16-bit or 8-bit 48/24/16/8 KHz PCM format

### Miscellaneous

- Use a single external 27MHz crystal to support both 960H and 720H video
- Two programmable PLLs integrated
- Slave I2C bus
- Ultra low power consumption. Under 500mW for normal operation. Under 50mW for suspend mode.
- 128-pin LQFP package (14mmx14mm)
- 1.8V core power, 3.3V analog power and 1.8V analog power

### Applications

Suggested applications include

- DVR
- Car DVR
- Video capture card

## Terminal Assignment

1	VDDA	97	VSS
2	AOUT	98	oCCIRD_0[7]
3	VSSA	99	oCCIRD_0[6]
4	VSSA	100	oCCIRD_0[5]
5	AINN	101	oCCIRD_0[4]
6	AIN1	102	VDDO
7	AIN2	103	oCCIRD_0[3]
8	AIN3	104	oCCIRD_0[2]
9	AIN4	105	oCCIRD_0[1]
10	AINS	106	oCCIRD_0[0]
11	VDDA	107	VSS
12	VDDV	108	CLKP01
13	INA0	109	CLKNO1
14	INB0	110	VDDI
15	VSSV	111	ACLKR
16	VSSV	112	ASYNR
17	INA1	113	ADATR
18	INB1	114	ADATM
19	VDDV	115	VSS
20	VDDV	116	ACLKP
21	INA2	117	ASTYNP
22	INB2	118	ADATP
23	AGND	119	IRQ
24	VSSV	120	VDDO
25	INA3	121	HRSTZ
26	INB3	122	ALINK0
27	VDDV	123	VSS
28	AVDD_1	124	MPP4
29	NC	125	MPP3
30	AVSS_1	126	MPP2
31	NC	127	MPP1
32	NC	128	VDDI
	SADD[0]	39	SIZCLK
	SADD[1]	38	SIZCD
	TEST_EN	37	VDDI
	AVSS_2	35	ALINK1
	NC	36	VSS
	AVDD_2	34	NC
	NC	33	VSS

## DM5866

128 Pin LQFP\_14x14

## Terminal Functions

### Analog Video/Audio Interface Pins

Pin Name	Pin number	Type	Description
INA0	13	A	CVBS input A of channel 0 or S-VIDEO Y of channel 0
INB0	14	A	CVBS input B of channel 0 or S-VIDEO Y of channel 0
INA1	17	A	CVBS input A of channel 1 or S-VIDEO C of channel 0
INB1	18	A	CVBS input B of channel 1 or S-VIDEO C of channel 0
INA2	21	A	CVBS input A of channel 2 or S-VIDEO Y of channel 1
INB2	22	A	CVBS input B of channel 2 or S-VIDEO Y of channel 1
INA3	25	A	CVBS input A of channel 3 or S-VIDEO C of channel 1
INB3	26	A	CVBS input B of channel 3 or S-VIDEO C of channel 1
AIN1	6	A	Audio input of channel 1
AIN2	7	A	Audio input of channel 2
AIN3	8	A	Audio input of channel 3
AIN4	9	A	Audio input of channel 4
AIN5	10	A	Audio input of channel 5
AINN	5	A	Audio input negative control
AOUT	2	A	Audio output

**Digital Video/Audio Interface Pins**

Pin Name	Pin number	Type	Description
oCCIRD_0[7:0]	98,99,100, 101,103,104 105,106	O	Video data output of channel 0 or TDM72/144 output Data Bus
oCCIRD_1[7:0]	85,86,87, 88,90,91, 92,93	O	Video data output of channel 1, or TDM72/144 output Data Bus
oCCIRD_2[7:0]	69,70,71, 72,74,75, 76,77	O	Video data output of channel 2
oCCIRD_3[7:0]	56,57,58, 59,61,62, 63,64	O	Video data output of channel 3
ACLKR	111	O	Audio serial clock output of record
ASYNR	112	O	Audio serial sync output of record.
ADATR	113	O	Audio serial data output of record
ADATM	114	O	Audio serial data output of mixing
ACLKP	116	O	Audio serial clock output of playback
ASYNP	117	O	Audio serial sync output of playback
ADATP	118	I	Audio serial data input of playback
ALINKI	40	I	Audio Multi-chip serial input
ALINKO	122	O	Audio Multi-chip serial output
MPP4	124	IO	FLD/ACTIVE/NOVID/FASTSW_SEL of channel 4
MPP3	125	IO	FLD/ACTIVE/NOVID/FASTSW_SEL of channel 3
MPP2	126	IO	FLD/ACTIVE/NOVID/FASTSW_SEL of channel 2
MPP1	127	IO	FLD/ACTIVE/NOVID/FASTSW_SEL of channel 1

**System Control Pins**

Pin Name	Pin number	Type	Description
HRSTZ	121	I	System reset
XI	82	I	Crystal 27MHz connection or Oscillator clock input.
XO	83	O	Crystal 27MHz connection
SADD[1:0]	38,39	I	I2C Device ID strapping
CLKPO1	108	O	36/72/144MHz clock output for oCCIRD_0
CLKNO1	109	O	Inverse of 36/72/144MHz clock output for oCCIRD_0
CLKPO2	95	O	36/72/144MHz clock output for oCCIRD_1
CLKNO2	96	O	Inverse of 36/72/144MHz clock output for oCCIRD_1
CLKPO3	79	O	36MHz clock output for oCCIRD_2
CLKNO3	80	O	Inverse of 36MHz clock output oCCIRD_2
CLKPO4	66	O	36MHz clock output for oCCIRD_3
CLKNO4	67	O	Inverse of 36MHz clock output for oCCIRD_3
TEST_EN	37	I	Test enable, please connect it to ground
SI2CD	42	IO	Slave I2C data
SI2CLK	43	I	Slave I2C clock
IRQ	119	O	Interrupt request output

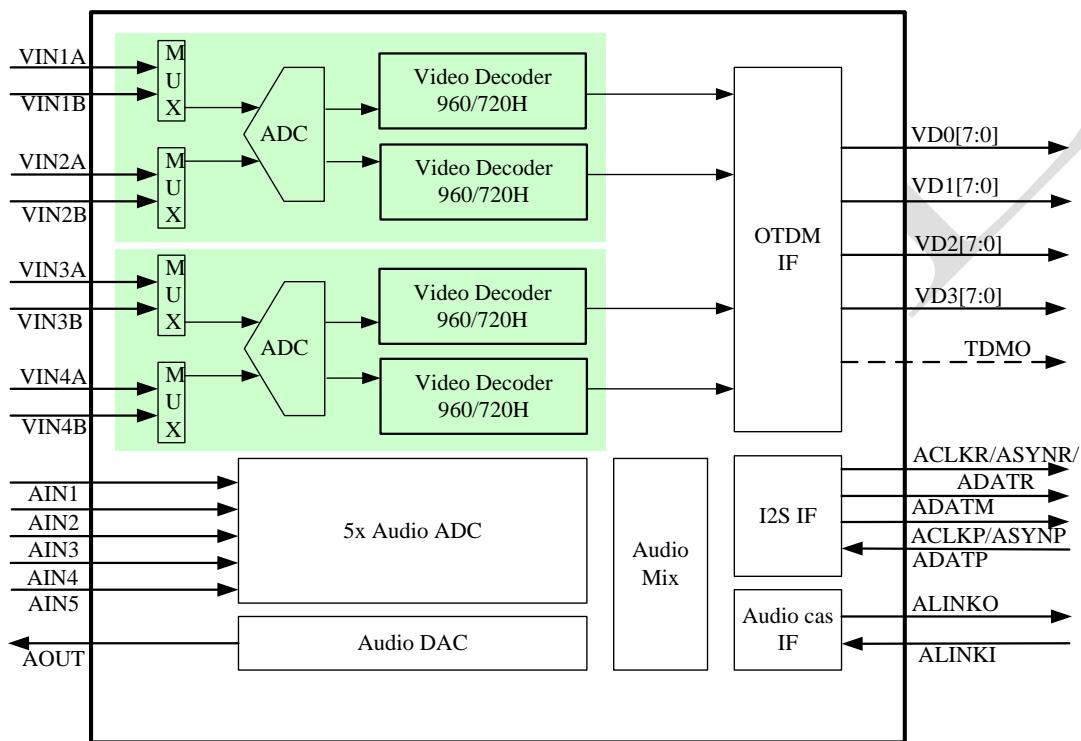
**Power, Ground and NC Pins**

Pin Name	Pin number	Type	Description
VDDA	1,11	P	1.8V Power for analog audio DAC
VSSA	3,4	G	Ground for analog audio DAC
VDDV	12,19,20,27	P	1.8V Power for video ADC
VSSV	15,16,24	G	Ground for video ADC
AGND	23	G	Analog ground (used as signal input reference, CH_AGND)
AVDD_1	28	P	1.8V Power for analog clock PLL1
AVSS_1	30	G	Ground for analog clock PLL1
AVDD_2	34	P	1.8V Power for analog clock PLL2
AVSS_2	35	G	Ground for analog clock PLL2
VDDI	41,60,78,94, 110,128	P	1.8V Power for internal logic
VDDO	53,68,84, 102,120	P	3.3V Power for output driver
VSS	36,44,55,65, 73,81,89,97, 107,115,123	G	Ground for internal logic and output driver
NC	29,31,32,33, 45,46,47,48, 49,50,51,52, 54		Not Connected

**Pin Usage of Video Output**

<b>Video Out</b>	1	oCCIRD_0[7:0] SD: CCIR656/TDM2/TDM4
	2	oCCIRD_1[7:0] SD: CCIR656/TDM2/TDM4
	3	oCCIRD_2[7:0] (Only for VD2) (Only SD CCIR656, No TDM out)
	4	oCCIRD_3[7:0] (Only for VD3) (Only SD CCIR656, No TDM out)
	5	(a) set CCIROPINOPT=1 (b) supporting SD: CCIR656/TDM2/TDM4
		Data Bus[7:0]: Pin no. {116, 117, 118, 119, 122, 124, 125, 127}

## Block Diagram

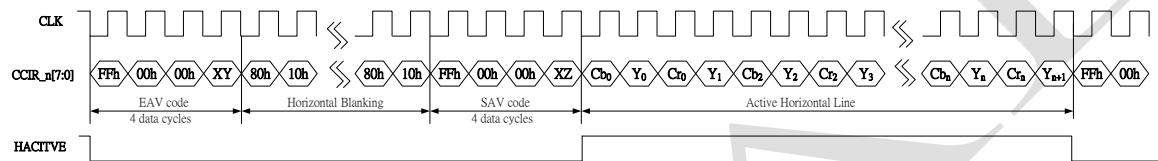


## Video Decoder

### Video Interface

The DM5866 outputs 27MHz CCIR656 with 720x480/720x576 resolution (conventional 720H), or outputs 36MHz CCIR656-like format (BT.1302) with 960x480/960x576 resolution (Sony 960H).

For these video outputs, SAV (Start of Active Video) and EAV (End of Active Video) are inserted to indicate active video interval. Each channel uses one output port to transmit video data, that is, luminance and chrominance data are transmitted through the same port. The output timing diagram is shown below.



The number of data cycles in active horizontal line will vary according to the output format. For 720H video outputs, the active horizontal line contains 1440 cycles. For 960 H video outputs, the active horizontal line contains 1920 cycles.

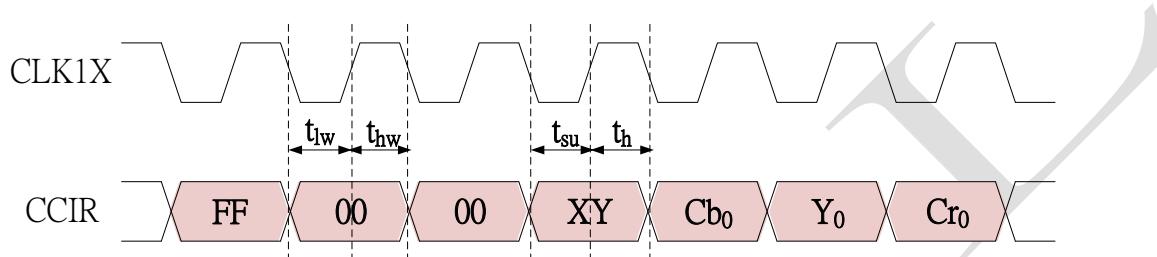
SAV and EAV indicate the active video interval. The values of the first three bytes in SAV and EAV are invariant preamble: 0xFF, 0x00, and 0x00. Different values are designated to the last byte according to different conditions: Field, V time, and H time. The MSB of this byte is always set to 1 and it's followed by three bits to represent the condition of F, V, and H respectively. The last four bits are used as protection bits. The detailed code sequences of SAV and EAV are illustrated in the following table.

Condition			FVH Value			SAV/EAV Code Sequence			
Field	V time	H time	F	V	H	Byte 0	Byte 1	Byte 2	Byte 3
Odd	Active	SAV	0	0	0	0xFF	0x00	0x00	0x80
Odd	Active	EAV	0	0	1	0xFF	0x00	0x00	0x9D
Odd	Blank	SAV	0	1	0	0xFF	0x00	0x00	0xAB
Odd	Blank	EAV	0	1	1	0xFF	0x00	0x00	0xB6
Even	Active	SAV	1	0	0	0xFF	0x00	0x00	0xC7
Even	Active	EAV	1	0	1	0xFF	0x00	0x00	0xDA
Even	Blank	SAV	1	1	0	0xFF	0x00	0x00	0xEC
Even	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xF1

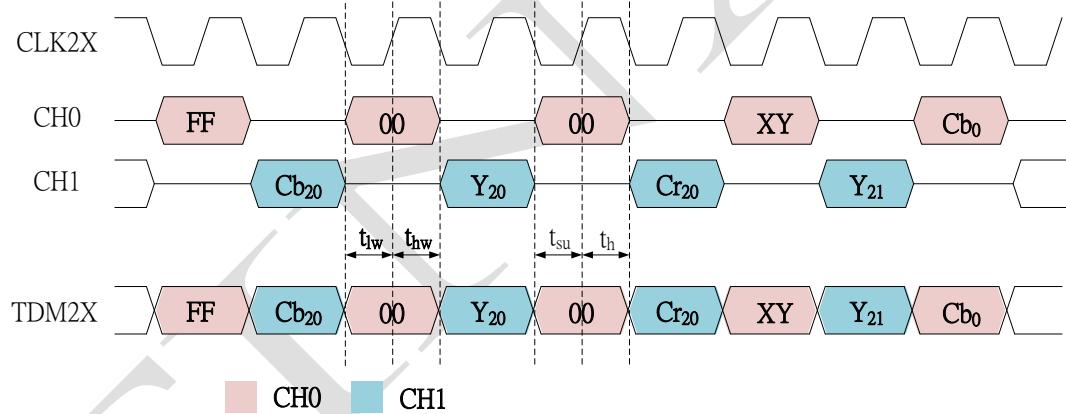
## Multi-channel Time Division Multiplexing

The DM5866 supports 2/4-channel time division multiplexed output format. Thus two or four video channels can be transmitted through one output port. The clock rate should be two or four times of the original sampling rate according to the number of channels to be multiplexed.

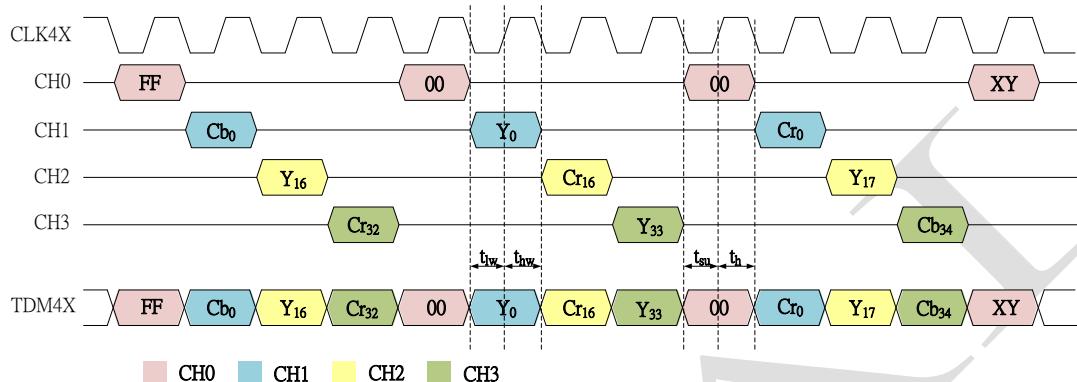
The basic case is the non-multiplexed output. The clock rate follows the original data rate (27 MHz for 720H video, 36 MHz for 960H video). The timing diagram is illustrated below.



When two-channel multiplexing is selected, two times of the original clock rate is used (54 MHz for 720H video, 72 MHz for 960H video). The timing diagram is illustrated below.



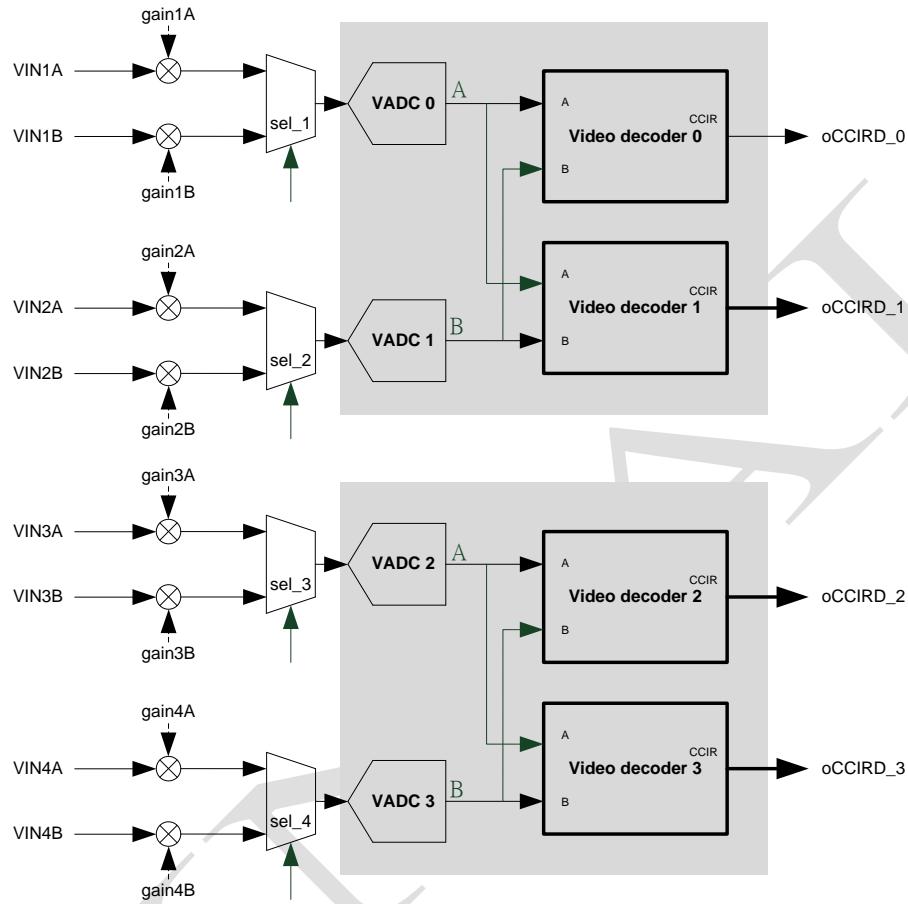
When four-channel multiplexing is selected, four times of the original clock rate is used (108 MHz for 720H video, 144 MHz for 960H video). The timing diagram is illustrated below.



In the Multi-channel Time Division Multiplexing mode, channel IDs are used to indicate the corresponding channels. Channel IDs are defined as the last four bits in SAV/EAV code sequence (i.e. the originally-defined protection bits). The relationship between SAV/EAV code sequence and channel ID is illustrated in the following table.

Condition			FVH Value			EAV/SAV Code Sequence						
Field	V time	H time	F	V	H	Byte 0	Byte 1	Byte 2	Byte 3			
			Ch0	Ch1	Ch2				Ch0	Ch1	Ch2	Ch3
Odd	Active	SAV	0	0	0	0xFF	0x00	0x00	0x80	0x81	0x82	0x83
Odd	Active	EAV	0	0	1	0xFF	0x00	0x00	0x90	0x91	0x92	0x93
Odd	Blank	SAV	0	1	0	0xFF	0x00	0x00	0xA0	0xA1	0xA2	0xA3
Odd	Blank	EAV	0	1	1	0xFF	0x00	0x00	0xB0	0xB1	0xB2	0xB3
Even	Active	SAV	1	0	0	0xFF	0x00	0x00	0xC0	0xC1	0xC2	0xC3
Even	Active	EAV	1	0	1	0xFF	0x00	0x00	0xD0	0xD1	0xD2	0xD3
Even	Blank	SAV	1	1	0	0xFF	0x00	0x00	0xE0	0xE1	0xE2	0xE3
Even	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xF0	0xF1	0xF2	0xF3

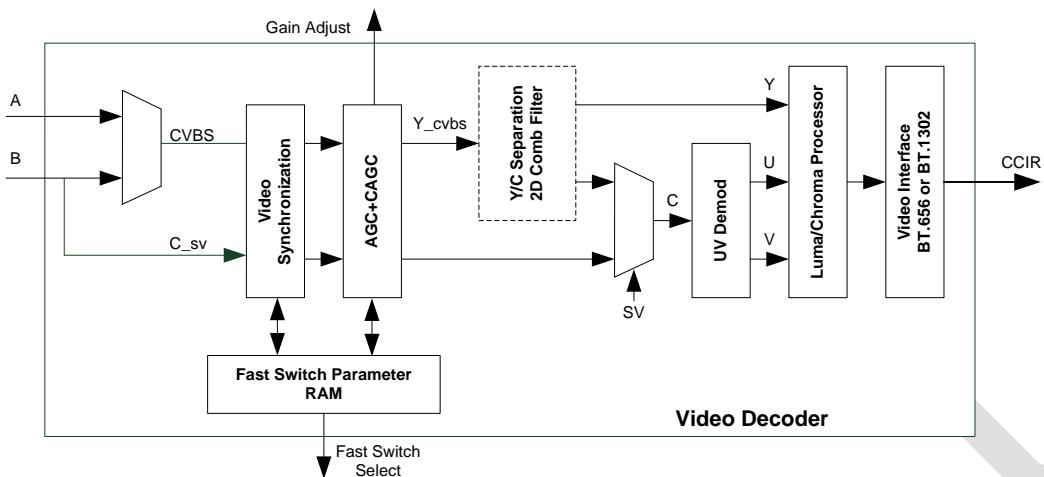
## 4-CH Video Decoder



The DM5866 contains four 960H/720H video decoders supporting up to 8 CVBS inputs.

Each CVBS has its own gain amplifier. For each pair of VINA and VINB, a 2-to-1 MUX selects one CVBS source and passes this source to one video analog-to-digital converter (VADC). The DM5866 has 4 VADCs and 4 video decoders (VD). The VADCs and VDs are organized as 2 banks as shown in the above figure. Each bank can be independently configured to operate at 27MHz (for 720H) or 36MHz (for 960H).

## Video Decoder Unit



The DM5866 video decoder contains a Video Synchronization block, an AGC block, an YC separation block, a UV Demodulation block, a Luma/Chroma Processor block and a BT 656 output block. A patented Fast Switch is also included.

In addition to CVBS, the DM5866 video decoder supports S-Video as well.

### Video Synchronization

Video Synchronization performs video detection function. It automatically detects NTSC(M), NTSC(443), PAL(B,D,G,H,I), PAL(M), PAL(N), PAL(60). A smart video detection algorithm has been adopted. Therefore the DM5866 can perform fast and stable video synchronization even if the input signal is weak or the external crystal is with error as large as +/- 1000 ppm.

### Automatic Gain Control

Automatic Gain Control (AGC) block performs both Luma AGC and Chroma AGC (CAGC). After video synchronization, Luma AGC adjusts input Luma level to the standard level (1Vpp). A further CAGC is performed after Luma AGC for signal with different Luma and Chroma attenuation.

## Y/C Separation

Y/C Separation is for CVBS input only. After this block CVBS signal is separated into Luma and Chroma components. A 5-H 2D comb filter is adapted in the Y/C separation block.

## UV demodulation

After Y/C separation, the UV demodulation block performs UV demodulation to the Chroma component. The phase and frequency of the UV demodulation is from a color burst subcarrier tracking block for both NTSC and PAL mode. A UV demodulation LPF is also adopted to filter out chroma noise.

## Luma/Chroma Processor

This block contains a programmable Luma sharpness filter. Hue, Saturation, Brightness and Contrast adjustment are also supported. The adjusted video is then transformed from YUV to YCbCr domain for CCIR656 output interface.

## Video Interface

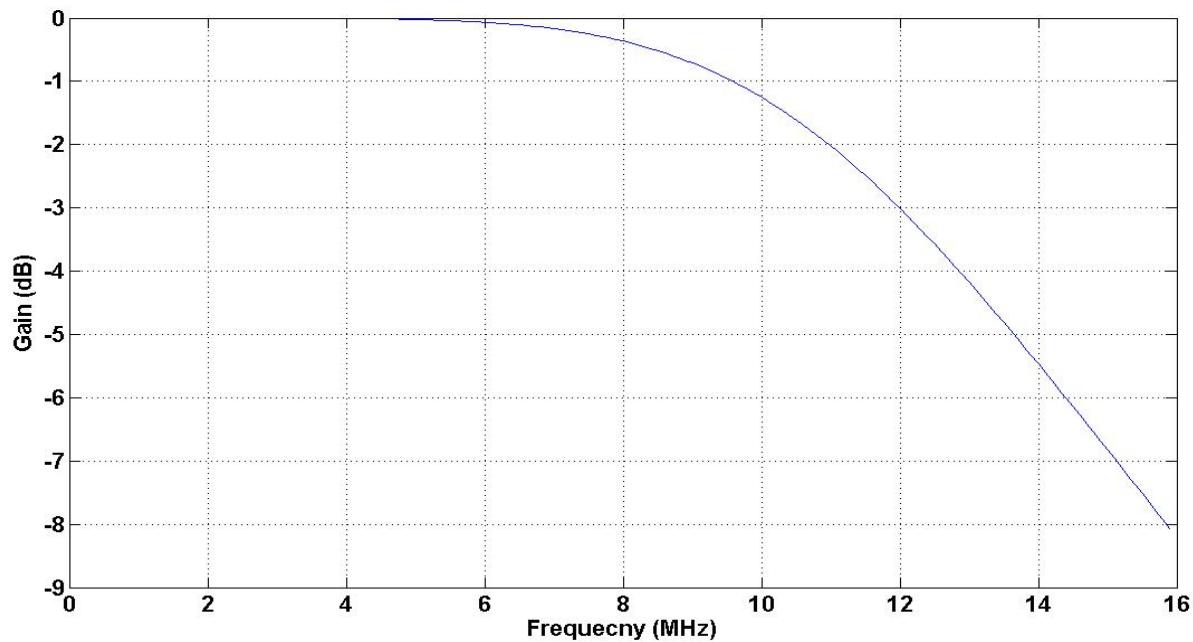
The DM5866 video decoder supports 27MHz BT.656 (for 720H) and 36MHz BT.656-like (for 960H) video output format. A horizontal cropping function also included in this block.

## Fast Switch Parameter RAM

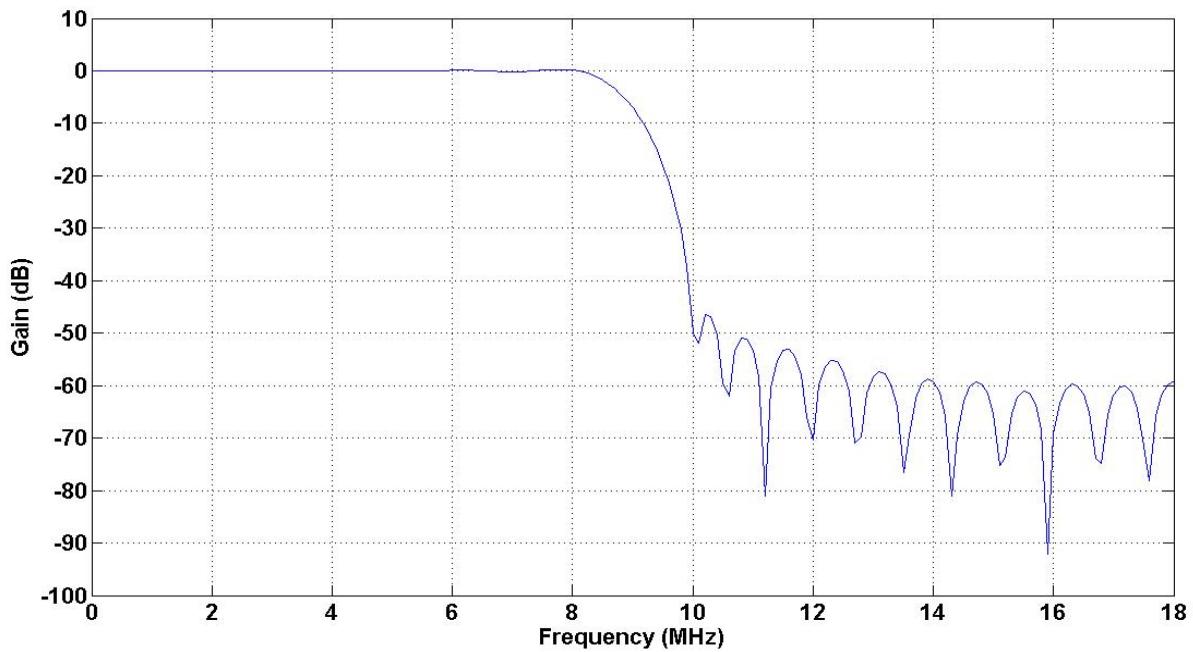
The DM5866 features a patented hardware video source fast switch function. The Fast Switch block has a table which stores video characteristic. Each time HW switches to a previously tracked video source it could complete video synchronization within several lines. With this feature, the DM5866 can decode up to 8 CVBS with little frame rate loss.

## Filter response

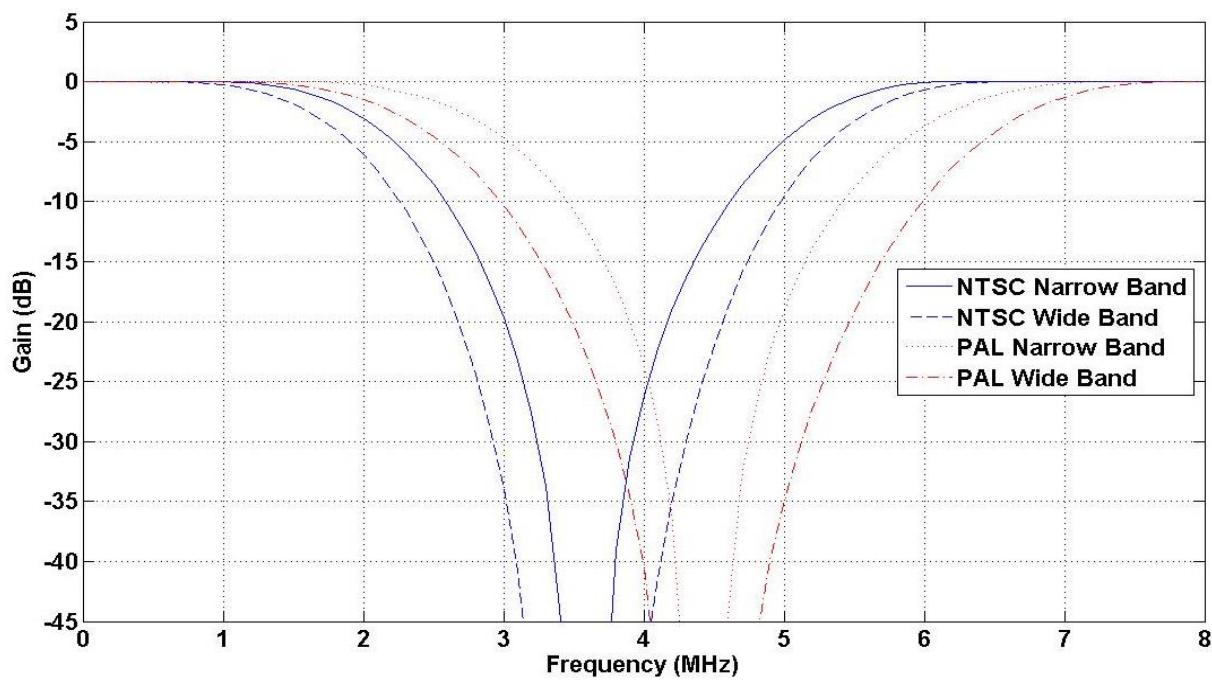
### Anti-alias LPF (960H)



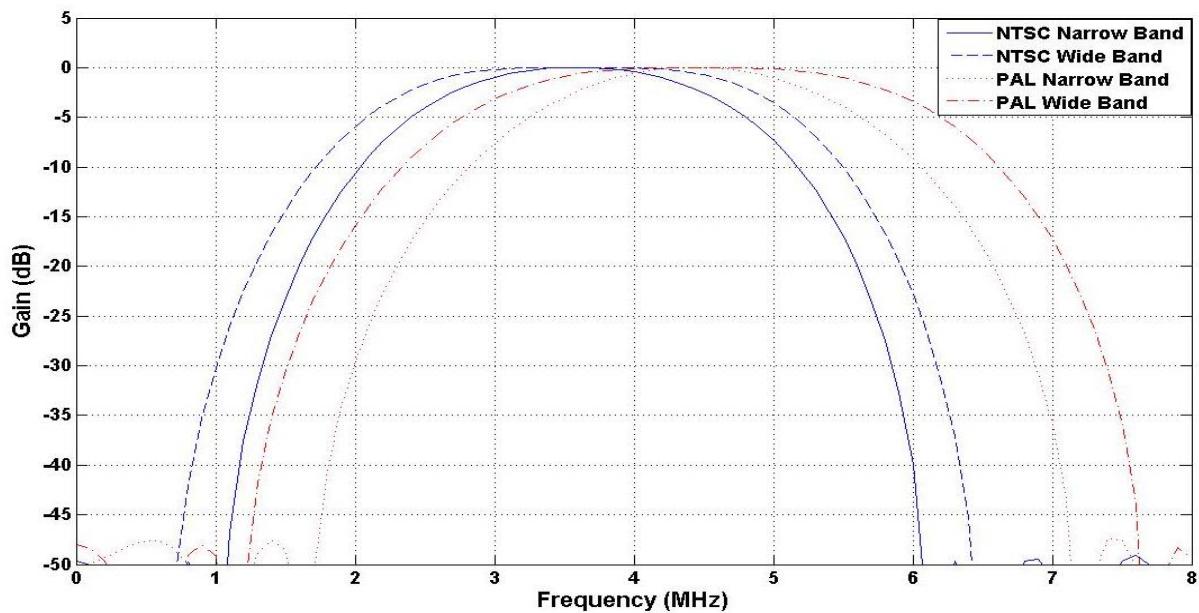
### Decimation filter (960H)



### Luma notch filter (960H)

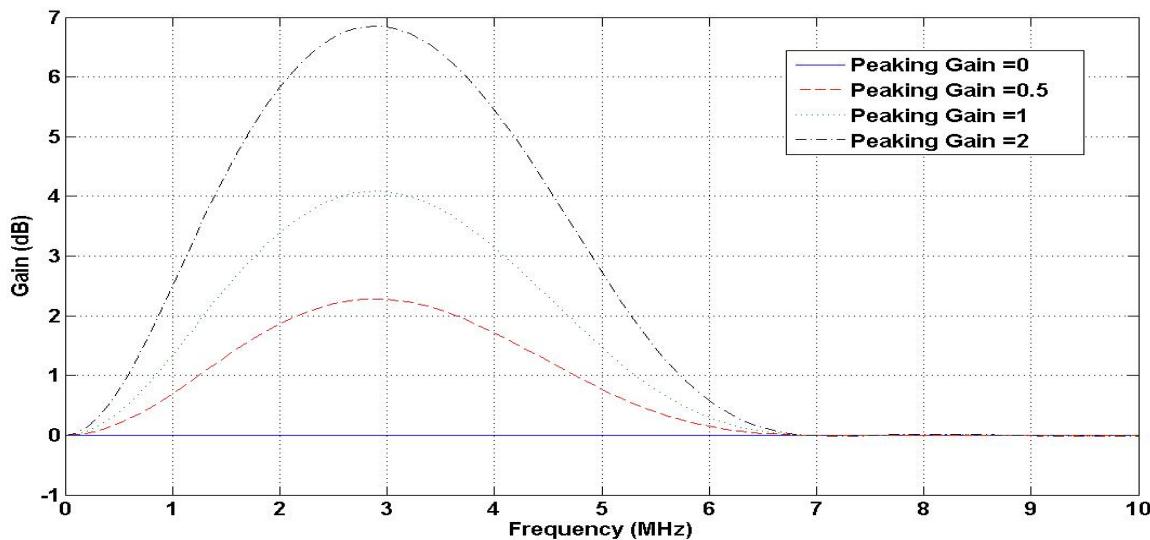


### Chroma band pass filter (960H)

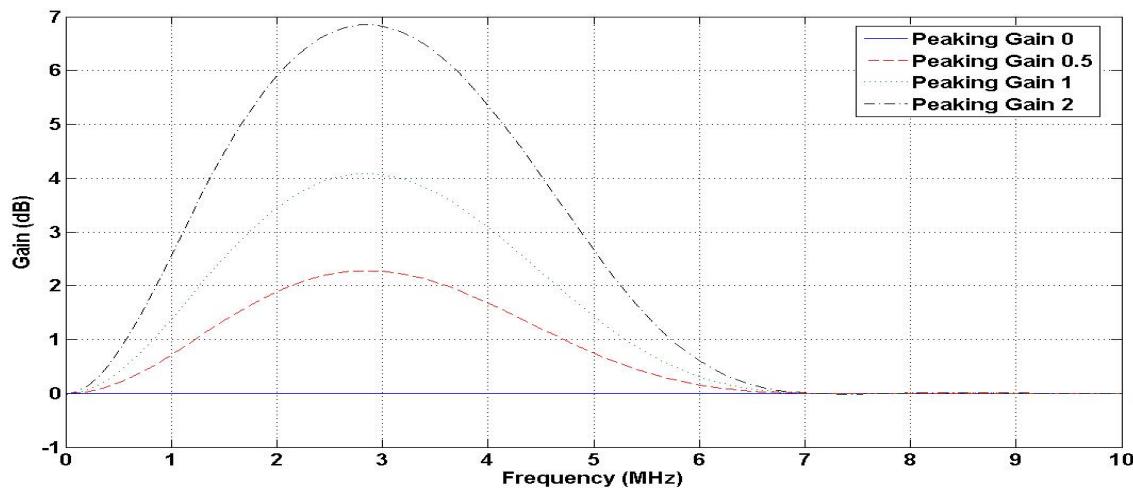


**Y sharpness filter (960H)**

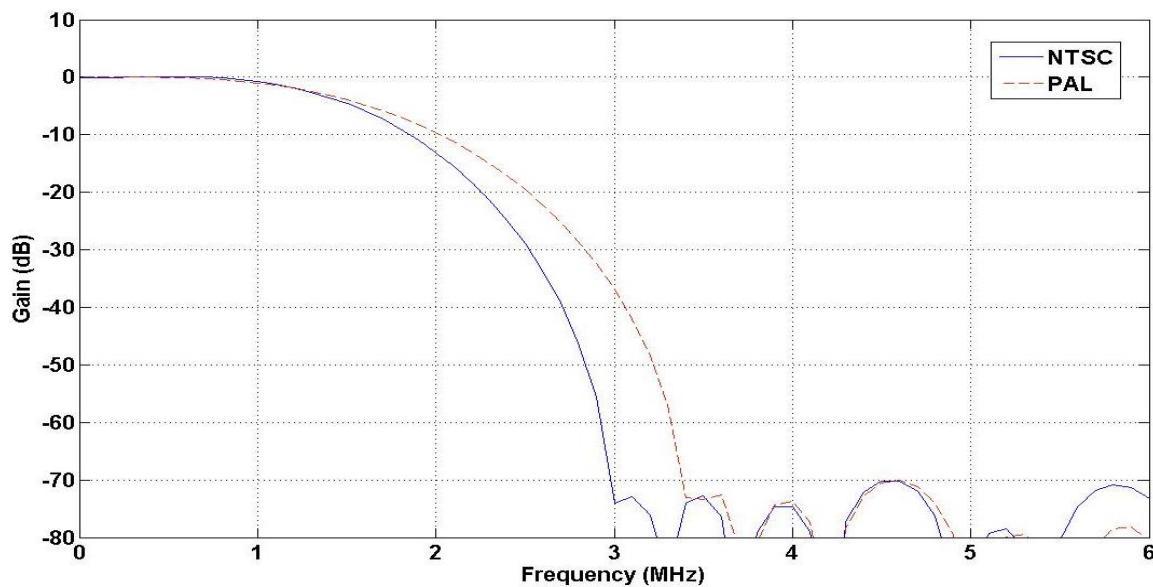
■ NSTC



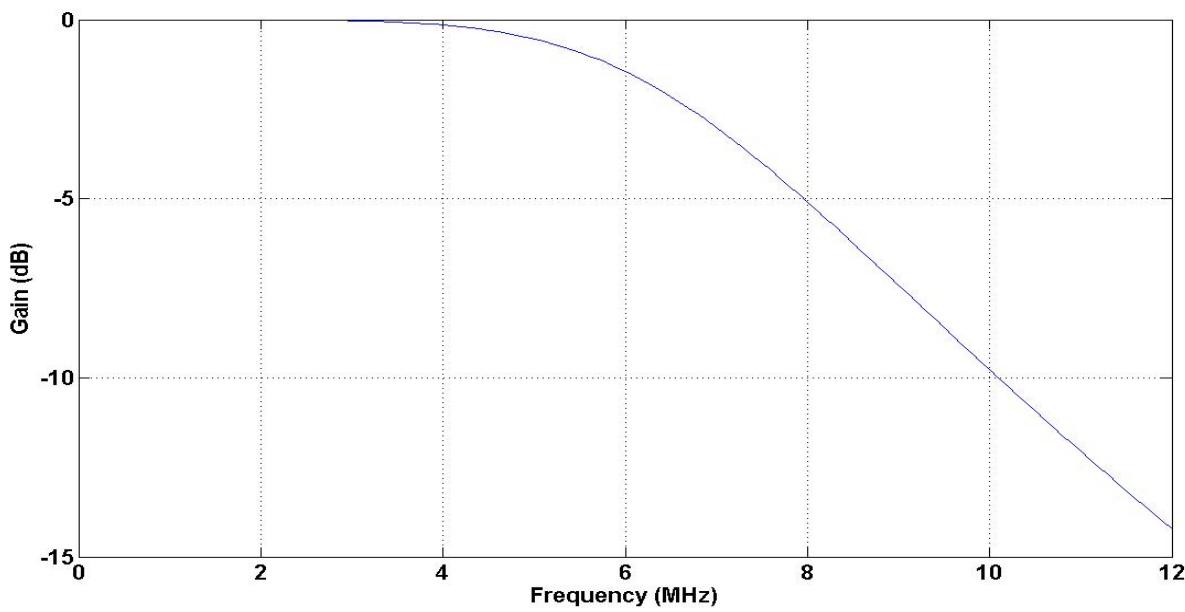
■ PAL



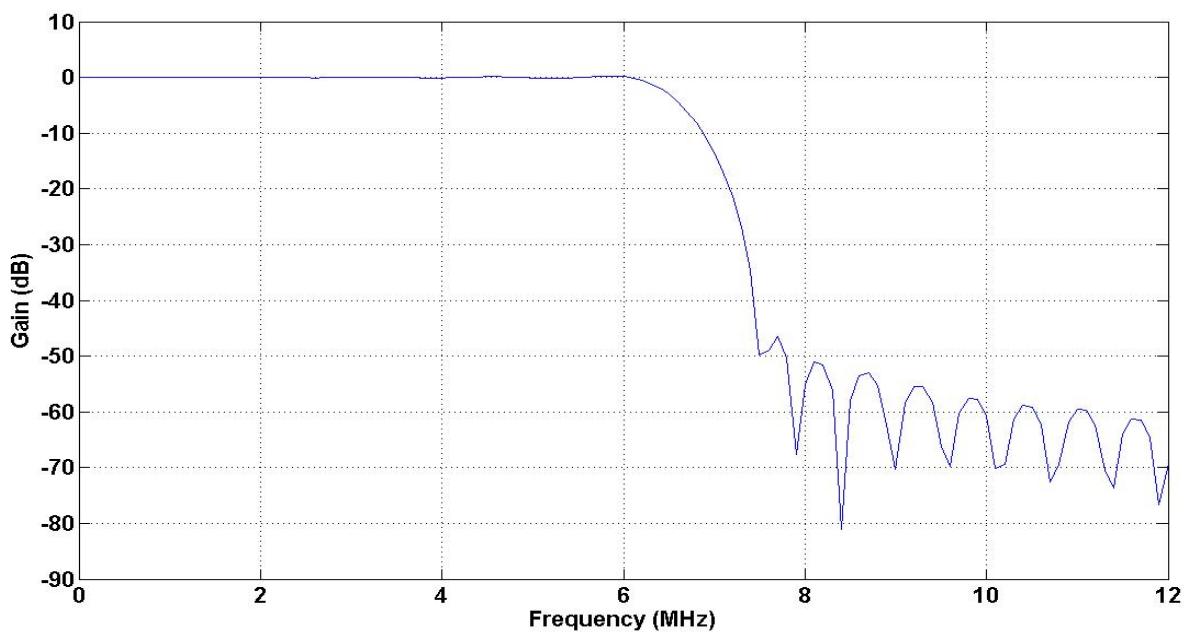
### UV demodulation low pass filter (960H)



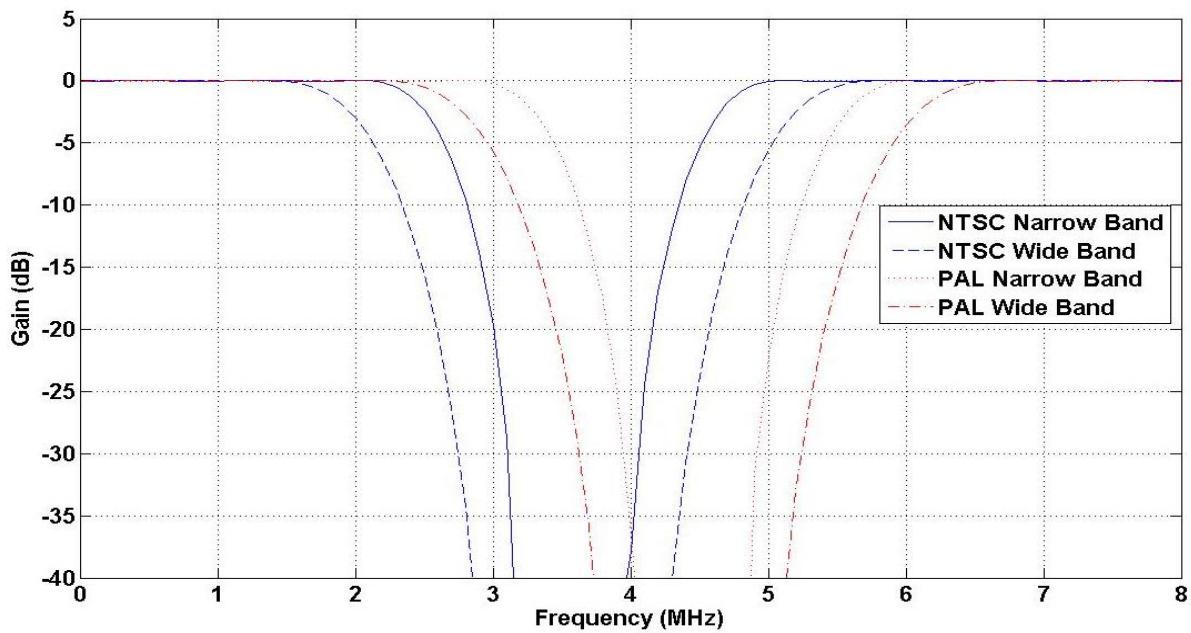
### Anti-alias LPF (720H)



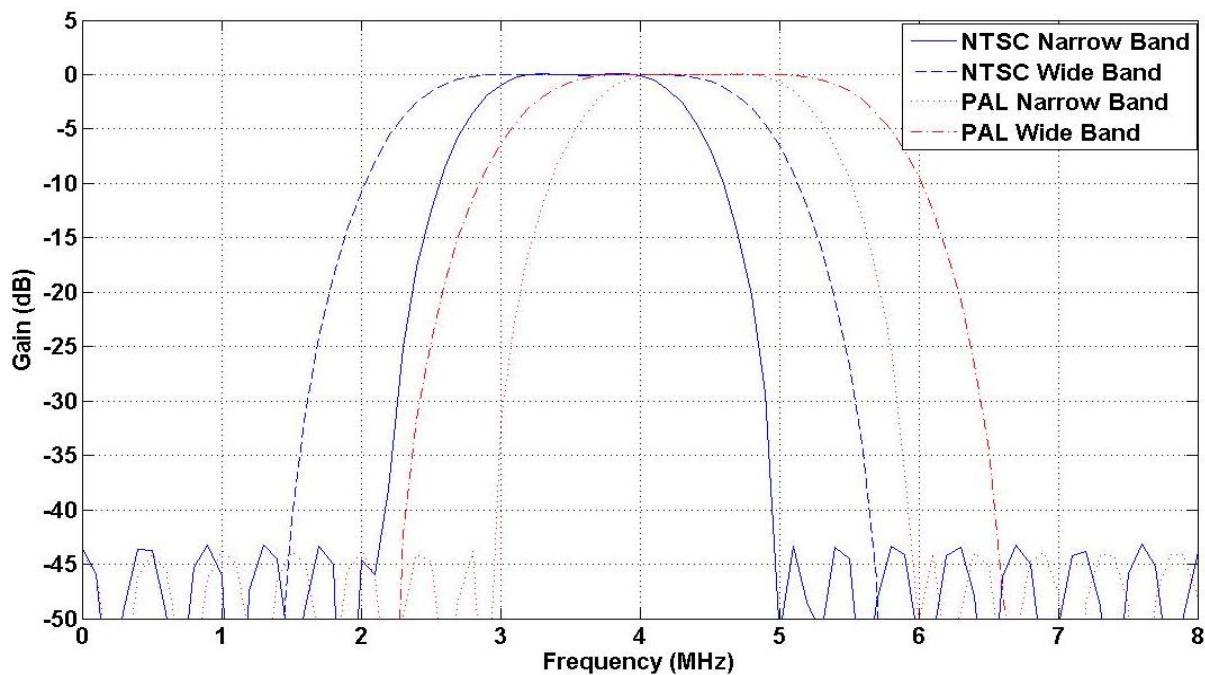
### Decimation filter (720H)



### Luma notch filter (720H)

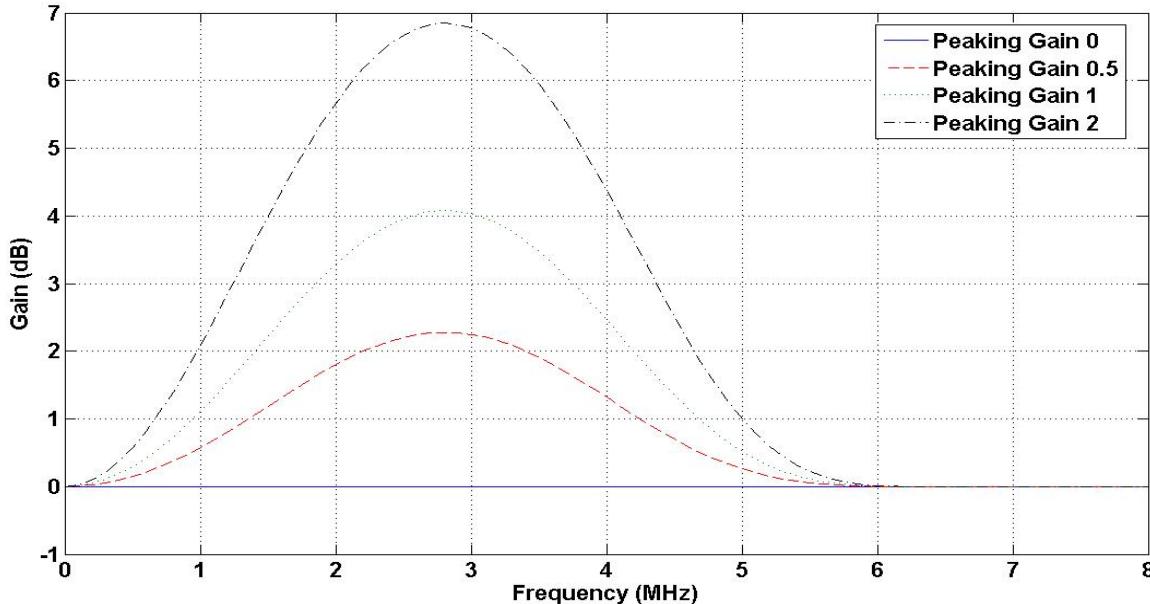


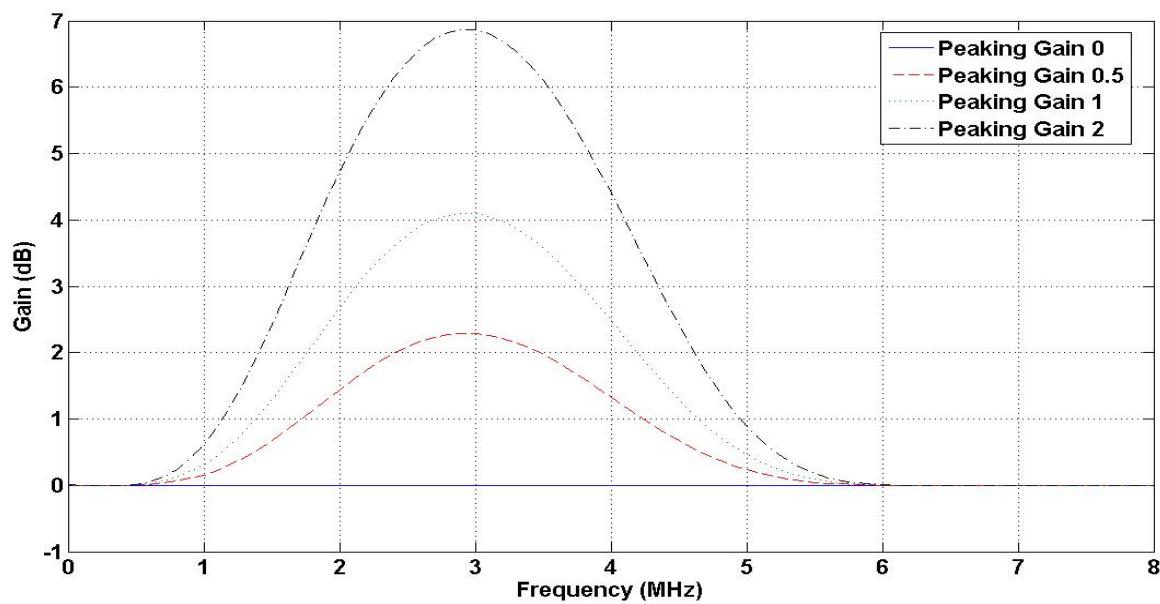
### Chroma band pass filter (720H)



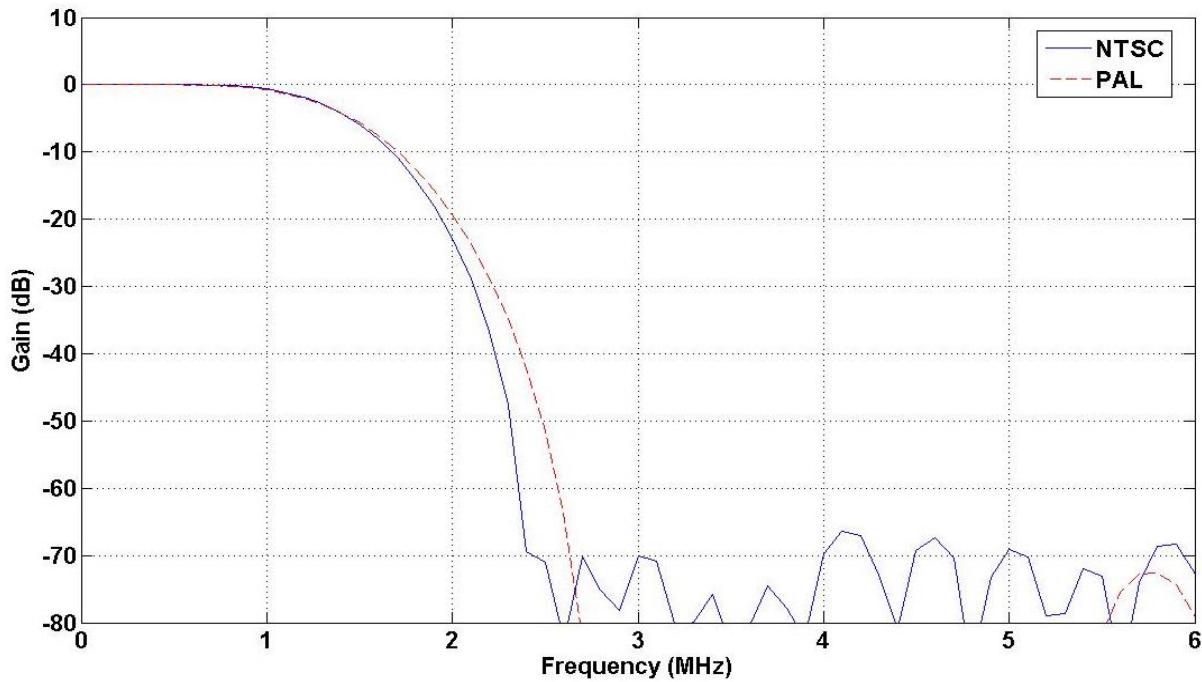
### Y sharpness filter (720H)

■ NTSC



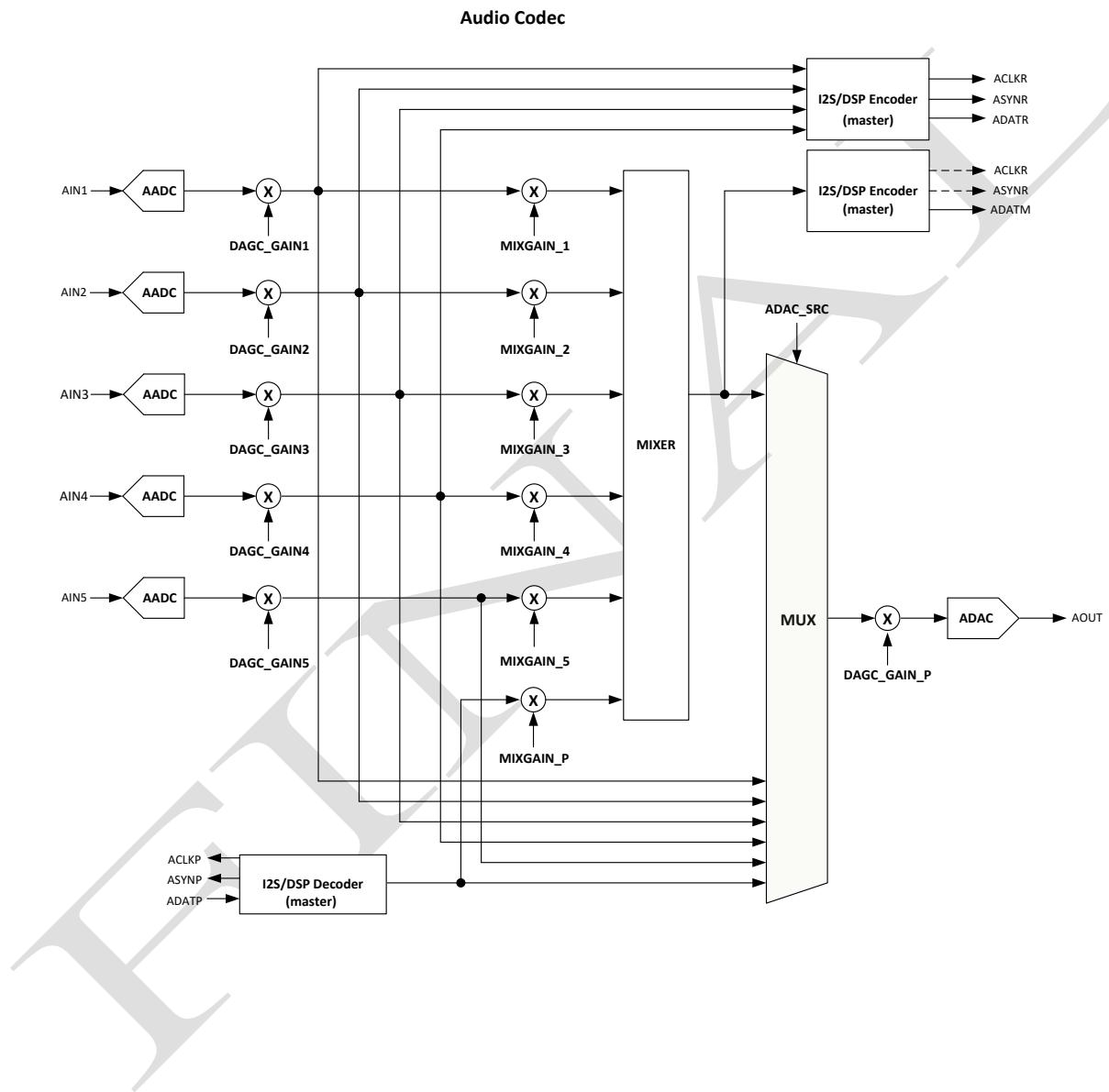
■ PAL


### UV demodulation low pass filter (720H)



## Audio CODEC

The audio codec in the DM5866 consists of five audio ADCs, one audio DAC, one audio mixer, one I2S/DSP decoder and two I2S/DSP encoders as shown below. The I2S/DSP decoder and encoders always operate in the master mode.



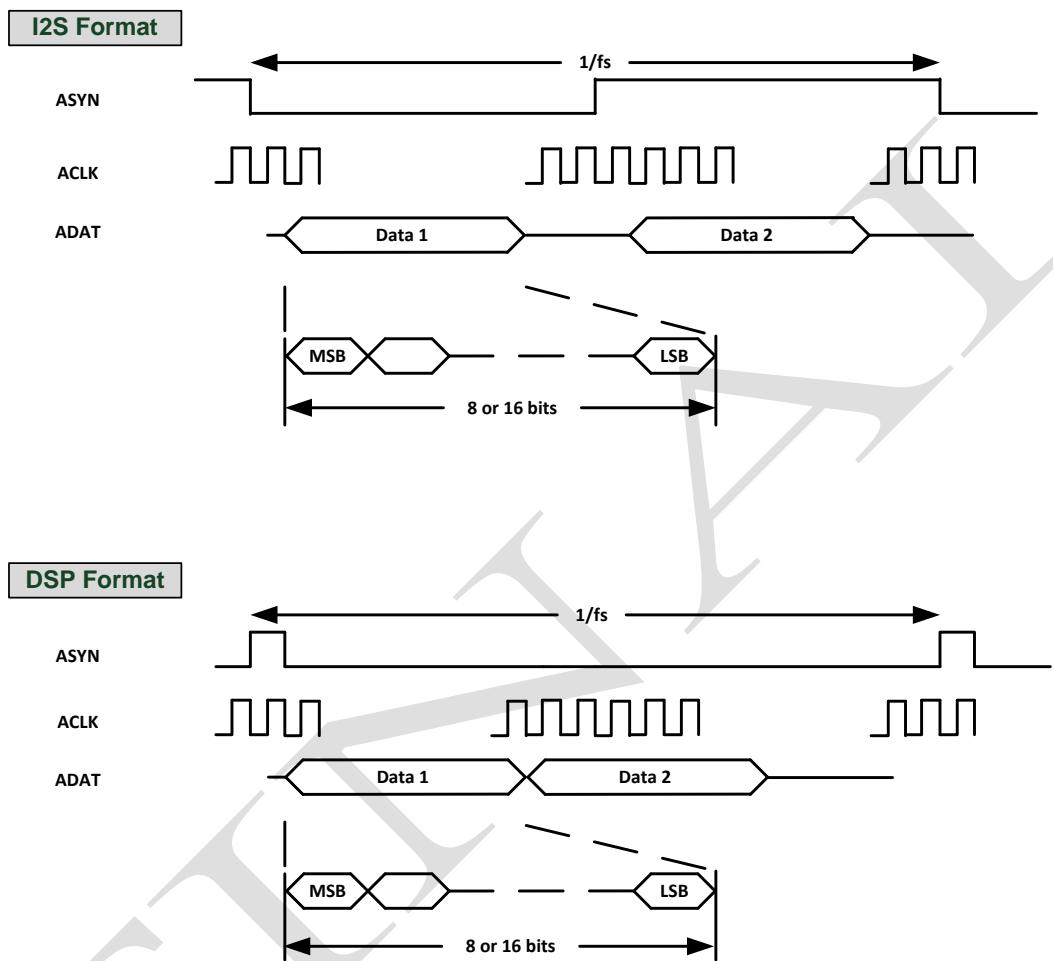
The I2S/DSP decoder is used for playback of digital input. It generates ACLKP and ASYNP signals and accepts serial data via ADATP from a slave device. The levels of the five analog audio inputs (AIN1 ~ AIN5) are programmable via the registers DAGC\_GAIN1, DAGC\_GAIN2, DAGC\_GAIN3, DAGC\_GAIN4 and DAGC\_GAIN5. The six input audio sources can be mixed by the user-defined ratio specified by registers MIXGAIN\_1, MIXGAIN\_2, MIXGAIN\_3, MIXGAIN\_4, MIXGAIN\_5, MIXGAIN\_P. The mixed audio can be output through I2S/DSP encoder or DAC.

The codec provides three interfaces for audio output. The audio DAC can output analog audio for any one of the six input audio sources or the mixed audio. The analog output level is adjustable via register DAGC\_GAIN\_P. Two I2S/DSP encoders are present to output digital audio signal. The first one generates ACLKR, ASYNR and ADATR to output the 4 recorded audio inputs. The second encoder uses ADATM and shares the other two signals (ACLKR and ASYNR) to output the mixed audio.

The codec also supports audio cascade mode for multi-chip operation which will be described in a dedicated section.

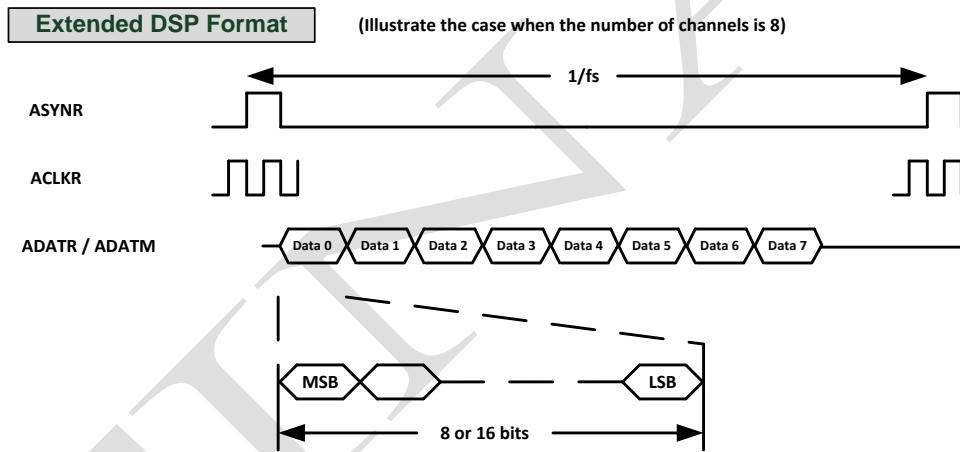
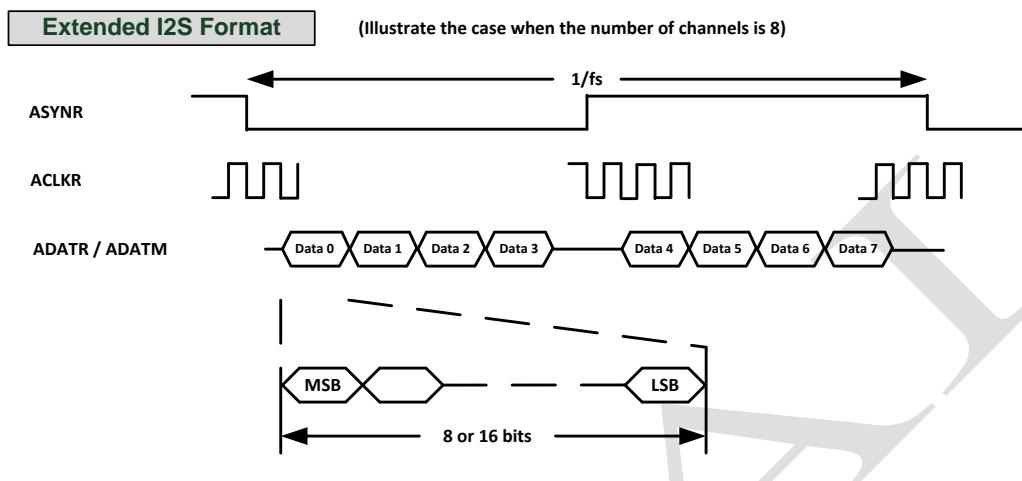
## Digital Audio Format

The 3 digital audio interfaces (decoder for playback and encoder for record or mixing) follow the standard I2S or DSP protocol as shown below. Only master mode (codec being the master) is supported.



## Extended Digital Audio Format

The digital audio encoders also support an extended I2S/DSP format to carry multiple audio channels through a single ADAT pin as shown below.



## Cascade Mode for Multi-Chip Operation

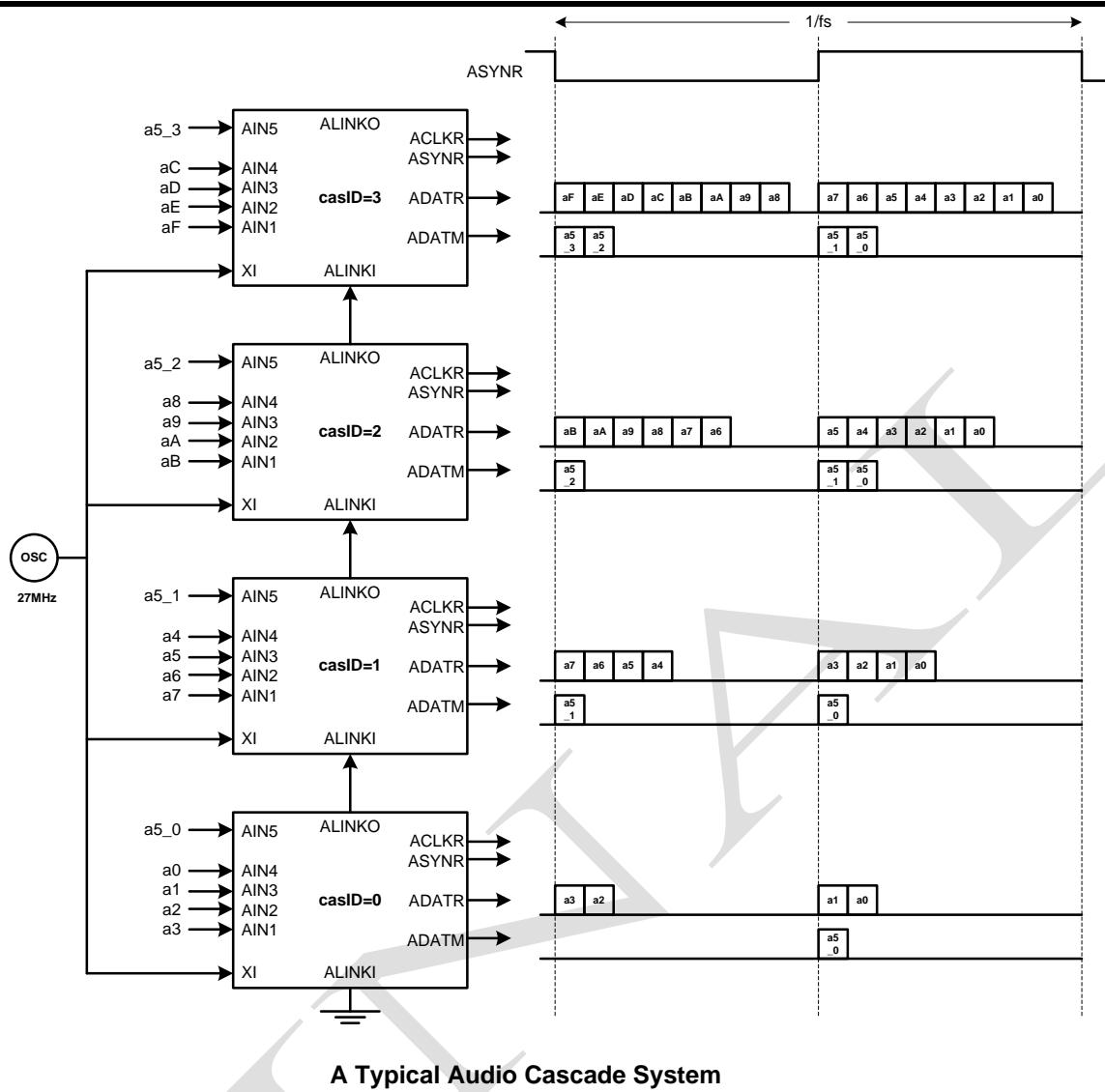
By using audio cascade mode, up to 16 analog audio sources can be cascaded and output through a single ACLKR/ASYNR/ADATR interface using the extended I2S/DSP format. Hence up to 4 chips can be cascaded in multi-chip application. A typical audio cascade system is shown below.

The table shown below summarizes the operation of audio cascade mode for various system configurations. Please note that 16-bit I2S/DSP data is not supported when using 16-channel cascade.

The analog audio input AIN5 can be optionally cascaded and output using the ADATM pin by setting the registers **MIXCASEN** and **ADATMOPT** as '1'.

	2-chip cascade (8 channels)		3-chip cascade (12 channels)		4-chip cascade (16 channels)	
	8-bit data	16-bit data	8-bit data	16-bit data	8-bit data	16-bit data
<b>fs=48KHz</b>	supported	supported	supported	supported	supported	<b>prohibited</b>
<b>fs=24KHz</b>	supported	supported	supported	supported	supported	<b>prohibited</b>
<b>fs=16KHz</b>	supported	supported	supported	supported	supported	<b>prohibited</b>
<b>fs=8KHz</b>	supported	supported	supported	supported	supported	<b>prohibited</b>

**The Operation of Audio Cascade Mode for Various System Configurations**


**<Note>**

1. Here we use I2S mode as an example. The DSP mode works accordingly.
2. The waveform is a simplified version.

In real system the “ASYNR” signals in different cascade stages are not synchronous.

## PLL

The DM5866 has two internal PLLs to generate the system and pixel clocks. A 27MHz or 36 MHz is required for the PLLs.

The default PLL setting is shown in the following table.

	<b>Crystal In clock (MHz)</b>	<b>PLL out (MHz)</b>	<b>Function</b>
<b>PLL1</b>	27	144	System/pixel clock
<b>PLL2</b>	27	74.25	SMPTE 274M pixel clock

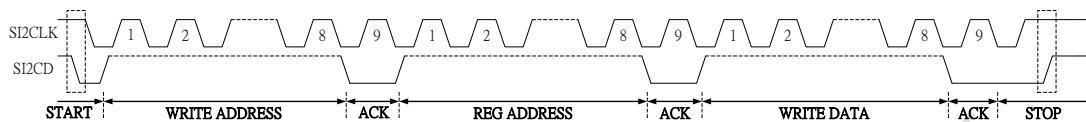
PLL default operated clock

The PLL parameters for various system configurations are shown in the following table.

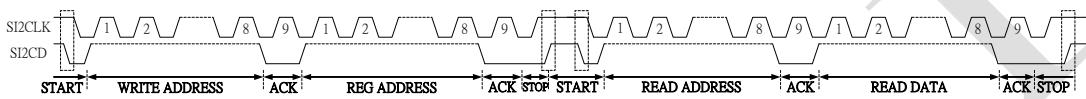
	<b>Crystal(MHz)</b>	<b>PLL out(MHz)</b>	<b>M</b>	<b>N</b>	<b>OD</b>
<b>PLL1</b>	27	144	64(62+2)	6(4+2)	1
	27	108	16(14+2)	2(0+2)	1
	36	144	16(14+2)	2(0+2)	1
	36	108	12(10+2)	2(0+2)	1
<b>PLL2</b>	27	144	64(62+2)	6(4+2)	1
	27	108	16(14+2)	2(0+2)	1
	27	74.25	22(20+2)	2(0+2)	2
	36	144	16(14+2)	2(0+2)	1
	36	108	12(10+2)	2(0+2)	1
	36	74.25	66(64+2)	8(6+2)	2

## Host Interface

In the DM5866, I<sup>2</sup>C is used for setting configuration and parameters, for example, brightness, contrast, saturation, hue, and sharpness control. The typical timing diagram of I<sup>2</sup>C write and read access is illustrated in the following figure.



Write operation of I<sup>2</sup>C bus



Read operation of I<sup>2</sup>C bus

Write/Read Address							
Slave Address						R/W	
1	1	0	0	0	SADD[1]	SADD[0]	0: Write; 1: Read

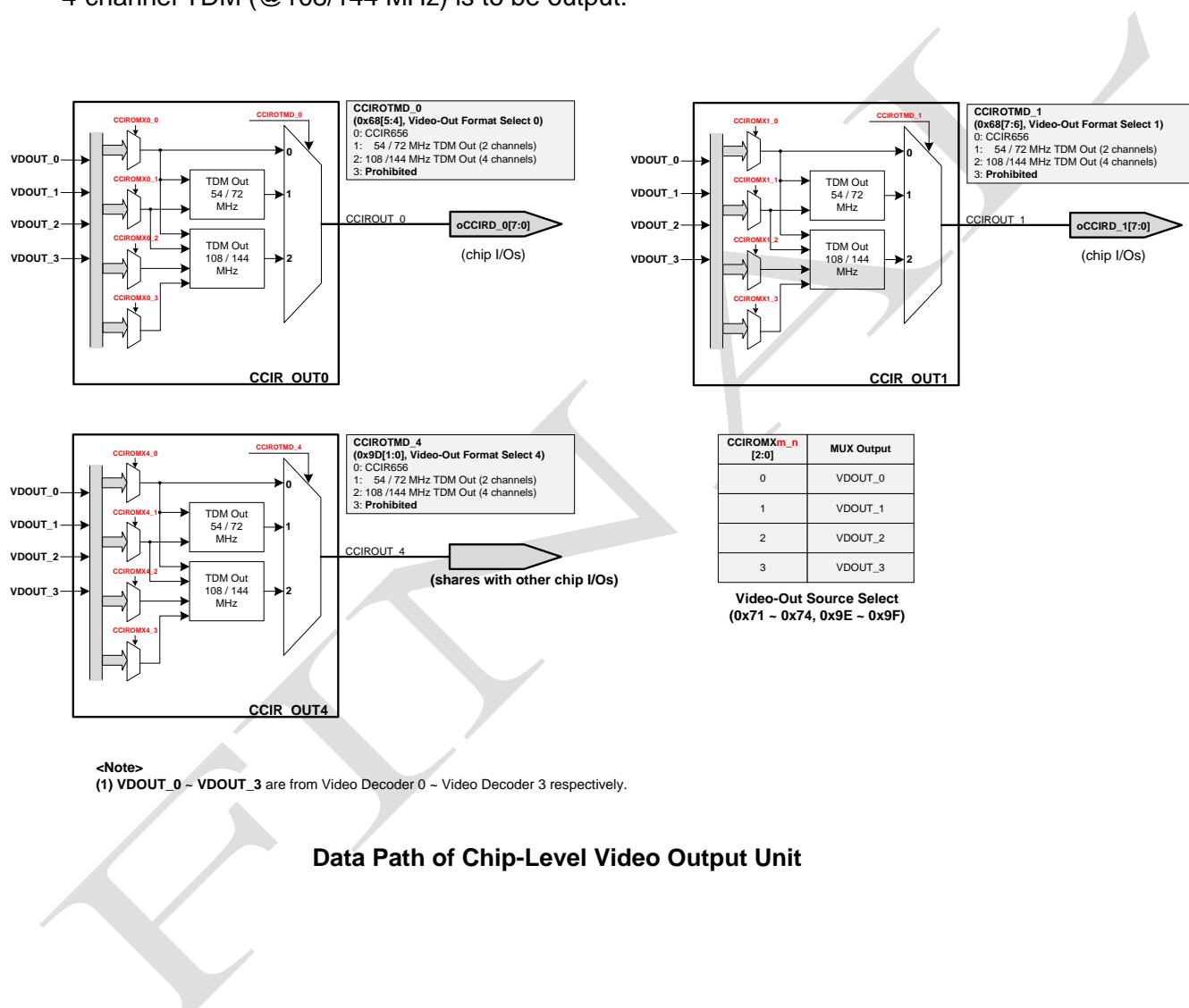
The external Pull-up/Pull-down resistors connected to the pins “DQ0” and “DQ1” indicate the device address SADD[1] and SADD[0]. When pull-up resistor is connected to DQ0 or DQ1, it indicates SADD[1] or SADD[0] with a high value. Otherwise when pull-down resistor is connected to DQ0 or DQ1, it indicates SADD[1] or SADD[0] with a low value.

	Write Address	Read Address
SADD[1:0]=2'h0	C0	C1
SADD[1:0]=2'h1	C2	C3
SADD[1:0]=2'h2	C4	C5
SADD[1:0]=2'h3	C6	C7

## Chip-Level Output Unit

Three video output ports are available at chip level. The following figure depicts the data path of output ports.

The output ports are flexible in use. It can be programmed to output various output combinations. As shown in the figure, the register **CCIROMX<sub>m</sub>\_n** is used to select up to 4 output videos from 6 possible sources. By programming register **CCIROTMD\_X**, user can specify whether single channel (CCIR656/BT.1302), 2-channel TDM (@54/72 MHz), 4-channel TDM (@108/144 MHz) is to be output.



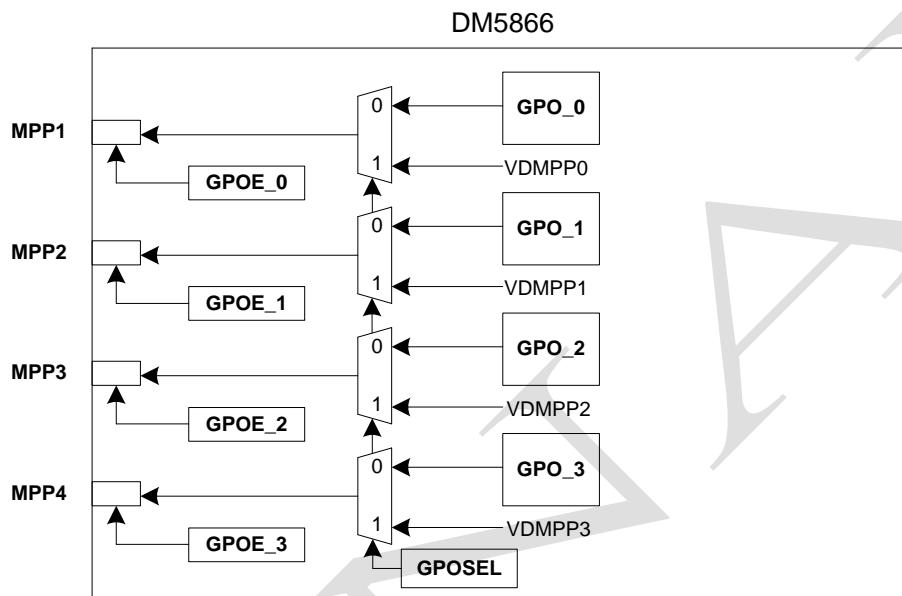
**CCIROUT\_0** and **CCIROUT\_1** have dedicated chip I/O pins (**oCCIRD\_0** and **oCCIRD\_1** respectively), while **CCIROUT\_4** has to share I/O pins with others. To use **CCIROUT\_4**, please set **CCIROPINOPT** as '1' and refer to the following table.

I/O Pin number	I/O Pin Name	CCIROUT_4 Bus
116	ACLKP	CCIROUT_4[7]
117	ASYNP	CCIROUT_4[6]
118	ADATP	CCIROUT_4[5]
119	IRQ	CCIROUT_4[4]
122	ALINKO	CCIROUT_4[3]
124	MPP4	CCIROUT_4[2]
125	MPP3	CCIROUT_4[1]
127	MPP1	CCIROUT_4[0]

## General Purpose Input /Output (GPIO)

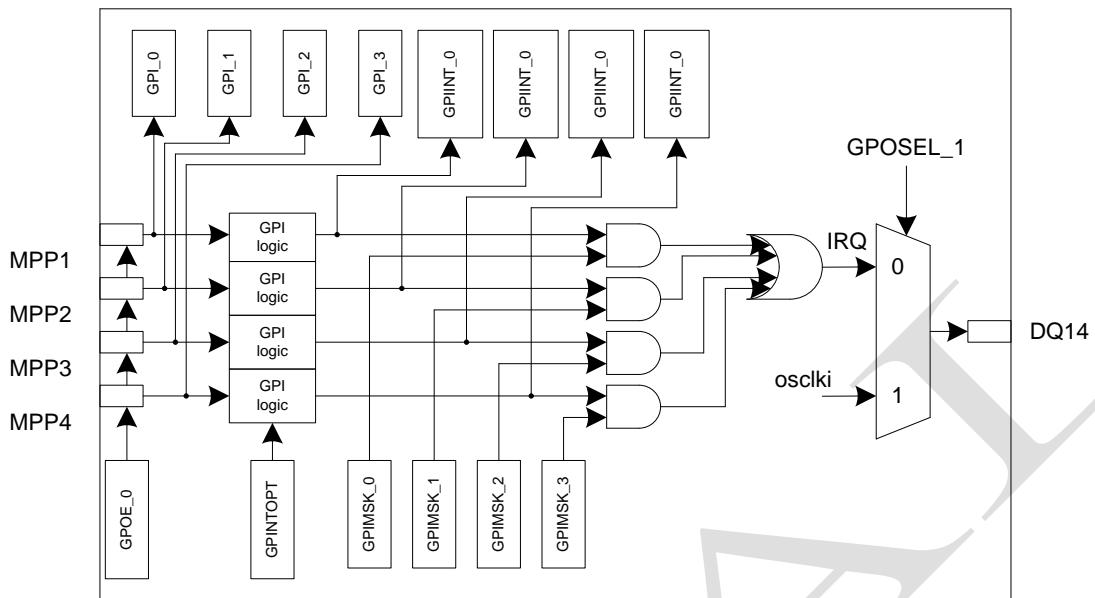
The DM5866 supports GPIO function. The function only valid when REG70 [4]=0 and REG7A[6]=0. REG7A~REG7F are corresponding GPIO registers and MPP1~MPP4 (pin No.127~24) are corresponding pins. We separate GPIO function into GPI and GPO for description. GPO function is used to set the programmable pin high or low by register. GPI function is used to detect the input signal high, low, raising edge or falling edge and then output high level signal to interrupt pin(IRQ). GPI and GPO are described below.

### GPO



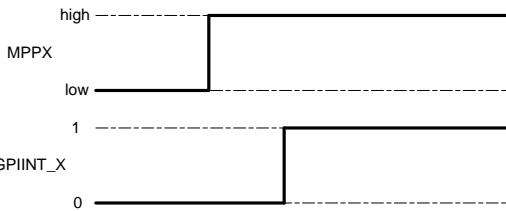
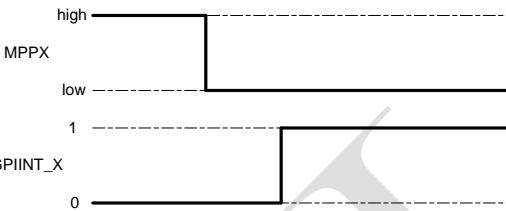
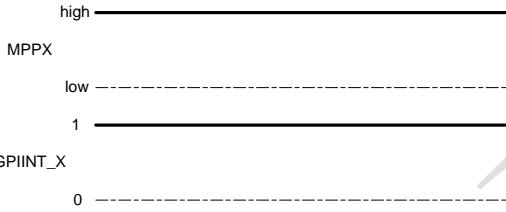
There are four GPO pin (MPP1~MPP4) in DM5866. The GPO function only valid when REG70[4]=0, REG7A[6]=0, **GPOSEL=0 (REG7A[7])** and **GPOE\_X=1 (REG7C[7:4])**. Fig.x shows the GPO function.

Pin MPP1~MPP4 can be programmed by GPO\_0~GPO\_3 (REG7C[3:0]) through GPO function.

**DM5866**


The DM5866 supports four GPI input pin and one IRQ output pin. Fig.x1 shows the GPI block diagram. The GPI function only valid when REG70[4]=0, REG7A[6]=0, **GPOE\_X=0 (REG7C[7:4])** and **GPOSEL\_1=0 (REG7A[4])**. The MPP1~MPP4 are the GPI input pin and DQ14 is the IRQ output pin. The GPI\_0~GPI\_3 are the read only status register. They show the GPI input from MPP1~MPP4 high or low. The GPIINT\_0~GPIINT\_3 are also read only status register. They show that GPI input MPP1~MPP4 high or low or raising edge or falling edge happened. The GPIINTOPT is the option to select GPI format from MPP1~MPP4 high or low or raising edge or falling edge. The GPIINTOPT table shows below. The GPIMSK\_0~GPIMSK\_3 are the mask signal for the corresponding GPI input.

**GPINTOPT table**

<b>GPINTOPT=2h0</b> Raising edge trigger 	<b>GPINTOPT=2h0</b> falling edge trigger 
<b>GPINTOPT=2h0</b> High level trigger 	<b>GPINTOPT=2h0</b> Low level trigger 

## Internal Control Registers

Note: Take 8'h64 for example – 8'= bit / h=hex / 64=value

### System Control

**Address= 8'h64**

System Control Page							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	1
				PAGE_3	PAGE_2	PAGE_1	PAGE_0

**PAGE\_0:** VD space 0, to access VD\_0 register please program this bit to 1.

**PAGE\_1:** VD space 1, to access VD\_1 register please program this bit to 1.

**PAGE\_2:** VD space 2, to access VD\_2 register please program this bit to 1.

**PAGE\_3:** VD space 3, to access VD\_3 register please program this bit to 1.

In case of register read, only one of the four bits can be set to 1.

**Address= 8'h65**

System Reset							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
						RSTZ	TRSTZ

**TRSTZ:** When 1, reset whole chip except SW PLL, GPIO and Device ID setting. (WO)

**RSTZ:** When 1, reset all video decoders, TDM and audio interface. It also resets video decoder configurations.

**Address= 8'h66**

Global INT Mask							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
				VDMAS K_3	VDMAS K_2	VDMAS K_1	VDMAS K_0

**VDMASK\_0:** Enable INT from VD\_0.

**VDMASK\_1:** Enable INT from VD\_1.

**VDMASK\_2:** Enable INT from VD\_2.

**VDMASK\_3:** Enable INT from VD\_3.

**Address= 8'h67**

Global INT Status							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
				VDINT_3	VDINT_2	VDINT_1	VDINT_0

**VDINT\_0:** VD\_0 INT status. (RO)

**VDINT\_1:** VD\_1 INT status. (RO)

**VDINT\_2:** VD\_2 INT status. (RO)

**VDINT\_3:** VD\_3 INT status. (RO)

**Address= 8'h68**

CCIR656 IO Control							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
2'h0		2'h0		0	0	0	0
CCIROTMD_1		CCIROTMD_0		CCIROE_3	CCIROE_2	CCIROE_1	CCIROE_0

**CCIROE\_0:** Chip CCIR656\_0 related 9 pins output enable.  
When 1, output mode. When 0, input mode.

**CCIROE\_1:** Chip CCIR656\_1 related 9 pins output enable.  
When 1, output mode. When 0, input mode.

**CCIROE\_2:** Chip CCIR656\_2 related 9 pins output enable.  
When 1, output mode. When 0, input mode.

**CCIROE\_3:** Chip CCIR656\_3 related 9 pins output enable.  
When 1, output mode. When 0, input mode.

**CCIROTMD\_0:** Chip CCUROUT\_0 output Mode type.

2'h0: CCIR656 output mode.

2'h1: 54/72Mhz TDM mode with D1 resolution for each channel.

2'h2: 108/144Mhz TDM mode with D1 resolution for each channel.

**CCIROTMD\_1:** Chip CCUROUT\_1 output Mode type.

2'h0: CCIR656 output mode.

2'h1: 54/72Mhz TDM mode with D1 resolution for each channel.

2'h2: 108/144Mhz TDM mode with D1 resolution for each channel.

**Address= 8'h69**

PIXCLK Polarity							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
OPIXCL K3_INV	OPIXCL K2_INV	OPIXCL K1_INV	OPIXCL K0_INV	OPIXCL K4_INV			

**OPIXCLK4\_INV:** When 1, inverse output pixclk of CCIROUT\_4.

**OPIXCLK0\_INV:** When 1, inverse output pixclk of CCIROUT\_0.

**OPIXCLK1\_INV:** When 1, inverse output pixclk of CCIROUT\_1.

**OPIXCLK2\_INV:** When 1, inverse output pixclk of CCIROUT\_2.

**OPIXCLK3\_INV:** When 1, inverse output pixclk of CCIROUT\_3.

**Address= 8'h6A**

IC Mode Control							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	2'h2		2'h0	
				PINCFG		CLKADCOPT	

**CLKADCOPT:** The VADC\_1 input clock selection. (144Mhz for 960H, 108MHz for 720H)

2'h0: The default value, sources from PLL1.

2'h1: Clock sources from PLL2.

2'h2: Clock source from chip pin NO.126.

**PINCFG:** IC pin mode option.

Set 2'h0 for 720 Video decoder x4.

Set 2'h2 for 960 Video decoder x4.

**Address= 8'h6B**

Output Pixclk Delay Configuration							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	3'h0			0	3'h0		
	DLYMUX_PIXCLK1				DLYMUX_PIXCLK0		

**DYLMUX\_PIXCLK0:** Programmable pixclk delay of CCIROUT\_0.

(3'h0: zero delay → 3'h7: max delay, add 0.6ns at every step)

**DYLMUX\_PIXCLK1:** Programmable pixclk delay of CCIROUT\_1.

(3'h0: zero delay → 3'h7: max delay, add 0.6ns at every step)

**Address= 8'h6C**

VD Power Down							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
				VDPWD_N_3	VDPWD_N_2	VDPWD_N_1	VDPWD_N_0

**VDPWDN\_0:** When 1, VD 0 into power down mode.

**VDPWDN\_1:** When 1, VD 1 into power down mode.

**VDPWDN\_2:** When 1, VD 2 into power down mode.

**VDPWDN\_3:** When 1, VD 3 into power down mode.

**Address= 8'h6D**

VD Power On Rstz							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
				VDPRST 3	VDPRST 2	VDPRST 1	VDPRST 0

**VDPRST0:** Write 1, reset VD 0.

**VDPRST1:** Write 1, reset VD 1.

**VDPRST2:** Write 1, reset VD 2.

**VDPRST3:** Write 1, reset VD 3.

**Address= 8'h6E**

IP Test Mode							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
VADCSEL		SW_VA DCBYP EN	SW_VA DCTSTE N	SW_PLL BYPEN	SW_PLL TSTEN	SW_MBI SPATEN	

**SW\_MBISTPATEN:** When 1, drive MBIST detail signal to chip IO pins.

**SW\_PLLTSTEN:** When 1, drive PLL out clocks to chip IO pins.

**SW\_PLLBYPEN:** When 1, bypass internal pll out source.

**SW\_VADCTSTEN:** When 1, drive VADCSEL indicated ADC outputs to chip IO pins.

**SW\_VADCBYPEN:** When 1, bypass VADCBYPOPT indicated ADC with chip input ADC signals.

**VADC\_SEL:** valid for SW\_VADCTSTEN

3'h0: VADC\_doutA=VADC\_dout1, VADC\_doutB=VADC\_dout2

3'h1: VADC\_doutA=VADC\_dout3, VADC\_doutB=VADC\_dout4

3'h2: VADC\_doutA= VADCMX0\_0 =>[VADC\_dout1/VADC\_dout2] mux

VADC\_doutA= VADCMX0\_1 =>[VADC\_dout3/VADC\_dout4] mux

3'h3: will drive VADC\_0 analog IP Do [15:1], selected signal to [VADC\_doutA, VADC\_doutB]

3'h4: will drive VADC\_1 analog IP Do [15:1], selected signal to [VADC\_doutA, VADC\_doutB]

**Address= 8'h6F**

MBIST Status							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
BISTGO	MBDON E		MBERR _4	MBERR _3	MBERR _2	MBERR _1	MBERR _0

**MBERR\_0:** When 1, memory of group 0 has error, Set by HW, write 1 to clear.

**MBERR\_1:** When 1, memory of group 1 has error, Set by HW, write 1 to clear.

**MBERR\_2:** When 1, memory of group 2 has error, Set by HW, write 1 to clear.

**MBERR\_3:** When 1, memory of group 3 has error, Set by HW, write 1 to clear.

**MBERR\_4:** When 1, memory of group 4 has error, Set by HW, write 1 to clear.

**MBDONE:** MBIST has finished self test, Set by HW, write 1 to clear.

**BISTGO:** Write 1to start MBIST logic. HW auto clear this bit after MBIST done.

**Address= 8'h70**

CCIROUT_4 Output Control							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
					CCIROP INOPT		

**CCIROPINOPT:** CCIROUT\_4 output

When set 1, enable CCIR656\_4 bus as output.

**Address= 8'h71**

CCIROUT_0 Otdm Configuration 1							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	3'h1			0	3'h0		
	CCIROMX0_1				CCIROMX0_0		

**CCIROMX0\_0:** The mux of CCIROUT\_0's channel 0 at OTDM mode.

**CCIROMX0\_1:** The mux of CCIROUT\_0's channel 1 at OTDM mode.

**Address= 8'h72**

CCIROUT_0 Otdm Configuration 2							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	3'h3			0	3'h2		
	CCIROMX0_3				CCIROMX0_2		

**CCIROMX0\_2:** The mux of CCIROUT\_0's channel 2 at OTDM mode.

**CCIROMX0\_3:** The mux of CCIROUT\_0's channel 3 at OTDM mode.

**Address= 8'h73**

CCIROUT_1 Otdm Configuration 1							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	3'h1			0	3'h0		
	CCIROMX1_1				CCIROMX1_0		

**CCIROMX1\_0:** The mux of CCIROUT\_1's channel 0 at OTDM mode.

**CCIROMX1\_1:** The mux of CCIROUT\_1's channel 1 at OTDM mode.

**Address= 8'h74**

CCIROUT_1 Otdm Configuration 2							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	3'h3			0	3'h2		
	CCIROMX1_3				CCIROMX1_2		

**CCIROMX1\_2:** The mux of CCIROUT\_1's channel 2 at OTDM mode.

**CCIROMX1\_3:** The mux of CCIROUT\_1's channel 3 at OTDM mode.

**Address= 8'h75**

IO/Clock Configuration							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
						ACLKP OE	ALINKO E
							IRQOE

**IRQOE:** If using DQ14 as IRQ, set this bit as '1'. Otherwise, this bit is "don't care"

**ALINKOE:** If audio data is to be sent to next stage using audio cascade mode, set as '1'.

Otherwise, set as '0'

**ACLKPOE:** Set as '1' when I2S playback is to be enabled.

**Address= 8'h77**

CHIP Status							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
							PWRON

**PWRON:** Power On status. (RO)

**Address= 8'h78**

I2C Master Configuration							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'hB8							
CH device address							

**CH0~CH3:** i2c slave device address. (R/W)

- DM5866 device address will be {4'hC,4'h0}
- I2CMaster\_0: device address will be {4'hC,4'h2}
- I2CMaster\_1: device address will be {4'hC,4'h4}
- I2CMaster\_2: device address will be {4'hC,4'h6}
- I2CMaster\_3: device address will be {4'hC,4'h8}
- For broadcast I2CMaster\_CH0~I2CMaster\_CH3, device address {4'HC,4'HE}

**Address= 8'h79**

I2CM status							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	2'h0		0	0	0	0
	MI2CRD CMD	MI2CSEL		CHNAC K3	CHNAC K2	CHNAC K1	CHNAC K0

**CHNACK0:** CH0 I2C fail (RO, WC) .

**CHNACK1:** CH1 I2C fail (RO, WC) .

**CHNACK2:** CH2 I2C fail (RO, WC) .

**CHNACK3:** CH3 I2C fail (RO, WC) .

**MI2CSEL:** The device address is 0xCA and select which channel will be set.

- I2CMaster\_CH0: device address will be {4'hC 4'ha} & {MI2CSEL=2'b00}.
- I2CMaster\_CH1: device address will be {4'hC 4'ha} & {MI2CSEL=2'b01}.
- I2CMaster\_CH2: device address will be {4'hC 4'ha} & {MI2CSEL=2'b10}.
- I2CMaster\_CH3: device address will be {4'hC 4'ha} & {MI2CSEL=2'b11}.

**MI2CRDCMD:** When 1, the MI2C restart command enable.

**Address= 8'h7A**

GPO Mode							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
GPOSE L	MI2CEN	MCLKO PT	GPOSE L_1				

**GPOSEL\_1:** Set 1, pin No.63 output oscski signal

Set 0, pin No.63 output IRQ function

**MCLKOPT:** When 1, fast master I2C clock speed.

**MI2CEN:** When 1, enable master I2C interface. (R/W)

**GPOSEL:** Set 1, pin MPP1 (pin No.127), MPP2 (pin No.126), MPP3(pin No.125), MPP4 (pin No.124) select VDMPP signal

Set 0, pin MPP1 (pin No.127), MPP2 (pin No.126), MPP3(pin No.125), MPP4 (pin No.124) select GPO signal

**Address= 8'h7C**

GPIO							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
<b>GPOE_3</b>	<b>GPOE_2</b>	<b>GPOE_1</b>	<b>GPOE_0</b>	<b>GPO_3</b>	<b>GPO_2</b>	<b>GPO_1</b>	<b>GPO_0</b>

**GPOE\_0:** GPO\_0 output enable

**GPOE\_1:** GPO\_1 output enable

**GPOE\_2:** GPO\_2 output enable

**GPOE\_3:** GPO\_3 output enable

**GPO\_0:** GPOSEL = 0 and GPOE\_0=1 Set 0 MPP1 output low, set 1 output high.

**GPO\_1:** GPOSEL = 0 and GPOE\_1=1 Set 0 MPP2 output low, set 1 output high.

**GPO\_2:** GPOSEL = 0 and GPOE\_2=1 Set 0 MPP3 output low, set 1 output high.

**GPO\_3:** GPOSEL = 0 and GPOE\_3=1 Set 0 MPP4 output low, set 1 output high.

**Address= 8'h7D**

GPIO							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
		<b>GPINTOPT</b>		<b>GPIMSK_3</b>	<b>GPIMSK_2</b>	<b>GPIMSK_1</b>	<b>GPIMSK_0</b>

**GPIMSK\_0:** GPI mask.

**GPIMSK\_1:** GPI mask.

**GPIMSK\_2:** GPI mask.

**GPIMSK\_3:** GPI mask.

**GPINTOPT:** GPI interrupt option

**Address= 8'h7E**

GPIO							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
<b>GPI_3</b>	<b>GPI_2</b>	<b>GPI_1</b>	<b>GPI_0</b>	<b>GPIINT_3</b>	<b>GPIINT_2</b>	<b>GPIINT_1</b>	<b>GPIINT_0</b>

**GPIINT\_0:** RO. GPI interrupt status register

**GPI\_0:** RO. GPI status register

**Address= 8'h7F**

SW FAST SWITCH							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
			OFASTS W_OPT	OFASTS W_SEL3	OFASTS W_SEL2	OFASTS W_SEL1	OFASTS W_SEL0

**OFASTW\_SEL0:**valid when VD0 REG04[4]=1 and OFASTSW\_OPT=1

set 0, select VIN1A as VD0 CVBS source

set 1, select VIN1B as VD0 CVBS source

**OFASTW\_SEL1:**valid when VD1 REG04[4]=1 and OFASTSW\_OPT=1

set 0, select VIN2A as VD1 CVBS source

set 1, select VIN2B as VD1 CVBS source

**OFASTW\_SEL2:**valid when VD2 REG04[4]=1 and OFASTSW\_OPT=1

set 0, select VIN3A as VD2 CVBS source

set 1, select VIN3B as VD2 CVBS source

**OFASTW\_SEL3:**valid when VD3 REG04[4]=1 and OFASTSW\_OPT=1

set 0, select VIN4A as VD3 CVBS source

set 1, select VIN4B as VD3 CVBS source

**OFASTSW\_OPT:** valid when REG04[4]=1

Set 0, VD0-VD3 SW FASTSW control signal from OFASTSW\_SEL0-OFASTSW\_SEL3

Set 1, VD0-VD3 SW FASTSW control signal from input pin MPP0~MPP3

## Video ADC

**Address= 8'h80**

Video ADC 0 Configuration 1							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
	<b>SW_sel_2</b>		<b>SW_sel_1</b>		<b>SWGAIN_0</b>	<b>pd_v2</b>	<b>pd_v1</b>

**pd\_v1:** Power down VIN1A & VIN1B, active high.

**pd\_v2:** Power down VIN2A & VIN2B, active high.

**SWGAIN\_0:** Software programs VADC 0's gain setting, active high. When low, the VADC 0' gain setting programmed by Hardware auto.

**SW\_sel\_1:** Software select active CVBS input. (0: VIN1A, 1: VIN1B)

**SW\_sel\_2:** Software select active CVBS input. (0: VIN2A, 1: VIN2B)

**Address= 8'h81**

Video ADC 0 Configuration 2							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			<b>4'hA</b>	0	0	0	0
			<b>bias_vadc12</b>	<b>SvideoC_2B</b>	<b>SvideoC_2A</b>	<b>SvideoC_1B</b>	<b>SvideoC_1A</b>

**bias\_vadc12:** VADC 0's bias setting.

**SvideoC\_1A:** Channel VIN1A chroma clamping. When 1, the analog clamping level is set to 50% for chroma signal processing.

**SvideoC\_1B:** Channel VIN1B chroma clamping. When 1, the analog clamping level is set to 50% for chroma signal processing.

**SvideoC\_2A:** Channel VIN2A chroma clamping. When 1, the analog clamping level is set to 50% for chroma signal processing.

**SvideoC\_2B:** Channel VIN2B chroma clamping. When 1, the analog clamping level is set to 50% for chroma signal processing.

**Address= 8'h82**

Video ADC 0 Configuration 3							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
<b>SW_gain1B</b>				<b>SW_gain1A</b>			

**SW\_gain1A:** VIN1A's gain value, valid when REG80[2]=1.

**SW\_gain1B:** VIN1B's gain value, valid when REG80[2]=1.

Ps. Minimum gain is set by 4'h0. Maximum gain is set by 4'hf.

The characteristic is the same as REG83

**Address= 8'h83**

Video ADC 0 Configuration 4							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
<b>SW_gain2B</b>				<b>SW_gain2A</b>			

**SW\_gain2A:** VIN2A's gain value, valid when REG80[2]=1.

**SW\_gain2B:** VIN2B's gain value, valid when REG80[2]=1.

**Address= 8'h84**

Video ADC 0 Configuration 5								
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit	
0	0	0	0	0	0	0	0	
Clmp1B				Clmp1A				

**Clmp1A:** VIN1A's clamp value.

**Clmp1B:** VIN1B's clamp value.

The clamp can be used to adjust the sync tip value to the nominal value of 20.

**Address= 8'h85**

Video ADC 0 Configuration 6								
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit	
0	0	0	0	0	0	0	0	
Clmp2B				Clmp2A				

**Clmp2A:** VIN2A's clamp value.

**Clmp2B:** VIN2B's clamp value.

**Address= 8'h86**

Video ADC 1 Configuration 1							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
	<b>SW_sel_4</b>		<b>SW_sel_3</b>		<b>SWGAIN_-1</b>	<b>pd_v4</b>	<b>pd_v3</b>

**pd\_v3:** Power down VIN3A & VIN3B, active high.

**pd\_v4:** Power down VIN3A & VIN3B, active high.

**SWGAIN\_1:** Software programs VADC 1's gain setting, active high. When low, the VADC 1' gain setting programmed by Hardware auto.

**SW\_sel\_3:** Software select active CVBS input. (0: VIN3A, 1: VIN3B)

**SW\_sel\_4:** Software select active CVBS input. (0: VIN4A, 1: VIN4B)

**Address= 8'h87**

Video ADC 1 Configuration 2							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			4'hA	0	0	0	0
			bias_vadc34	SvideoC_4B	SvideoC_4A	SvideoC_3B	SvideoC_3A

**bias\_vadc34:** VADC 1's bias setting.

**SvideoC\_3A:** Channel VIN3A chroma clamping. When 1, the analog clamping level is set to 50% for chroma signal processing.

**SvideoC\_3B:** Channel VIN3B chroma clamping. When 1, the analog clamping level is set to 50% for chroma signal processing.

**SvideoC\_4A:** Channel VIN4A chroma clamping. When 1, the analog clamping level is set to 50% for chroma signal processing.

**SvideoC\_4B:** Channel VIN4B chroma clamping. When 1, the analog clamping level is set to 50% for chroma signal processing.

**Address= 8'h88**

Video ADC 1 Configuration 3							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
SW_gain3B				SW_gain3A			

**SW\_gain3A:** VIN3A's gain value, valid when REG86[2]=1.

**SW\_gain3B:** VIN3B's gain value, valid when REG86[2]=1.

**Address= 8'h89**

Video ADC 1 Configuration 4							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
<b>SW_gain4B</b>				<b>SW_gain4A</b>			

**SW\_gain4A:** VIN4A's gain value, valid when REG86[2]=1.

**SW\_gain4B:** VIN4B's gain value, valid when REG86[2]=1.

**Address= 8'h8A**

Video ADC 1 Configuration 5							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
<b>Clmp3B</b>				<b>Clmp3A</b>			

**Clmp3A:** VIN3A's clamp value.

**Clmp3B:** VIN3B's clamp value.

**Address= 8'h8B**

Video ADC 1 Configuration 6							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
<b>Clmp4B</b>				<b>Clmp4A</b>			

**Clmp4A:** VIN4A's clamp value.

**Clmp4B:** VIN4B's clamp value.

**Address= 8'h8C**

Video ADC LPF Option							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	2'h0		2'h0	
				lpf_34		lpf_12	

**lpf\_12:** VADC 0 LPF selected.

**lpf\_34:** VADC 1 LPF selected.

**lpf\_xx:** 2'h0: 6MHz

2'h1: 9MHz

Others: bypass

**Address= 8'h8D**

VADC Clk Delay Configuration 1							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0		3'h0		0		3'h0	
	DLYMUX_ANA34				DLYMUX_ANA12		

**DLYMUX\_ANA12:** Programmable delay of digcore aclk\_out0 from aclk\_0.

(3'h0: zero delay → 3'h7: max delay, add 0.6ns at every step)

**DLYMUX\_ANA34:** Programmable delay of digcore aclk\_out1 from aclk\_1.

(3'h0: zero delay → 3'h7: max delay, add 0.6ns at every step)

**Address= 8'h8E**

VADC Clk Delay Configuration 2							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	3'h0			0	3'h0		
	DLYMUX_ANA72				DLYMUX_ANA36		

**DLYMUX\_ANA36:** Programmable delay of digcore aclk36\_out from aclk36.

(3'h0: zero delay → 3'h7: max delay, add 0.6ns at every step)

**DLYMUX\_ANA72:** Programmable delay of digcore aclk72\_out from aclk72.

(3'h0: zero delay → 3'h7: max delay, add 0.6ns at every step)

**Address= 8'h8F**

VADC Digcore Config							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	3'h0		
					DLYMUX_VD		

**DLYMUX\_VD:** Programmable delay of VD clk.

(3'h0: zero delay → 3'h7: max delay, add 0.6ns at every step)

## PLL

**Formula:**

$$\text{CLK\_OUT} = \text{XIN} * (\text{M}+2)/[(\text{N}+2)*\text{OD}*2]$$

Where CLK\_OUT: PLL output frequency

XIN: PLL input frequency.

M: The numerator of PLL formula.

[N, OD]: The denominator of PLL formula.

**Attention:**

1.  $100\text{MHz} \leq \text{CLK\_OUT} * \text{OD} \leq 250\text{MHz}$
2.  $1\text{MHz} \leq \text{XIN}/(\text{N}+2) \leq 25\text{MHz}$
3.  $\text{OD} \geq 1$

**Truth Table:**

PD	BP	OE	CLK_OUT
0	0	0	CLK_OUT
0	0	0	XIN
Don't Care	1	0	XIN
Don't Care	Don't Care	1	0
Other			Undefined

**PD:** Power down control; Active high.

**BP:** Bypass XIN to CLK\_OUT; Active high.

**OE:** CLK\_OUT enable pin, Active low.

**Address= 8'h90**

SW PLL Control							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
<b>SWPLL RST</b>						<b>SWPLL2</b>	<b>SWPLL1</b>

**SWPLL1:** set PLL1 input configuration from SWPLL1\_XX set, otherwise hard wired with chip default vale. (144MHz)

**SWPLL2:** set PLL2 input configuration from SWPLL2\_XX set, otherwise hard wired with chip default vale. (74.25MHz)

**SWPLLRST:** set 1, chip will enter a reset mode waiting for PLL stable in 1ms. After that, SW needs to re-program all register setting except PLL configuration.

**Address= 8'h91**

SW PLL Config							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
		<b>SWPLL2 _OE</b>	<b>SWPLL1 _OE</b>	<b>SWPLL2 _PD</b>	<b>SWPLL2 _BP</b>	<b>SWPLL1 _PD</b>	<b>SWPLL1 _BP</b>

**SWPLL1\_BP:** PLL1\_BP SW program source.

**SWPLL1\_PD:** PLL1\_PD SW program source.

**SWPLL2\_BP:** PLL2\_BP SW program source.

**SWPLL2\_PD:** PLL2\_PD SW program source.

**SWPLL1\_OE:** PLL1\_OE SW program source.

**SWPLL2\_OE:** PLL2\_OE SW program source.

**Address= 8'h92**

SWPLL1_M							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h0							
SWPLL1_M[7:0]							

**SWPLL1\_M:** PLL1\_M SW program source.

**Address= 8'h93**

SWPLL1_N							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0					5'h0
SWPLL1_M[8]							SWPLL1_N

**SWPLL1\_N:** PLL1\_N SW program source

**Address= 8'h94**

SWPLL2_M							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h0							
SWPLL2_M[7:0]							

**SWPLL2\_M:** PLL2\_M SW program source

**Address= 8'h95**

SWPLL2_N							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	<b>5'h0</b>				
<b>SWPLL2_M[8]</b>			<b>SWPLL2_N</b>				

**SWPLL2\_N:** PLL2\_N SW program source

**Address= 8'h96**

SWPLL_OD							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
<b>4'h0</b>				<b>4'h0</b>			
<b>SWPLL2_OD</b>				<b>SWPLL1_OD</b>			

**SWPLL1\_OD:** PLL1\_OD SW program source

**SWPLL2\_OD:** PLL2\_OD SW program source

DM5866 PLL SETTINGS Ref: 27MHz						
Ref: 27MHz	M	N	OD	PD	OE	BP
144 MHz	62	4	1	0	0	0
108 MHz	14	0	1	0	0	0
74.25 MHz	20	0	2	0	0	0

DM5866 PLL SETTINGS Ref: 36MHz						
Ref: 36MHz	M	N	OD	PD	OE	BP
144 MHz	14	0	1	0	0	0
108 MHz	10	0	1	0	0	0
74.25 MHz	64	6	2	0	0	0

**Address= 8'h9D**

CCIROUT_4 Output Control							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	3'h0			0	0	2'h0	
	DLYNUX_PIXCLK4					CCIROTMMD_4	

**DYLMUX\_PIXCLK4:** Programmable pixclk delay of CCIR656\_4.

(3'h0: zero delay → 3'h7: max delay, add 0.6ns at every step)

**CCIROTMMD\_4:** Chip CCIROUT\_4 output Mode type.

2'h0: CCIR656 output mode.

2'h1: 54/72Mhz TDM mode with D1 resolution for each channel.

2'h2: 108/144Mhz TDM mode with D1 resolution for each channel.

**Address= 8'h9E**

CCIROUT_4 Otdm Configuration 1							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	3'h0			0	3'h0		
	CCIROMX4_1					CCIROMX4_0	

**CCIROMX4\_0:** The mux of CCIR656\_4's channel 0 at OTDM mode.

**CCIROMX4\_1:** The mux of CCIR656\_4's channel 1 at OTDM mode.

**Address= 8'h9F**

CCIROUT_4 Otdm Configuration 2							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	3'h0			0	3'h0		
	CCIROMX4_3				CCIROMX4_2		

**CCIROMX4\_2:** The mux of CCIR656\_4's channel 0 at OTDM mode.

**CCIROMX4\_3:** The mux of CCIR656\_4's channel 2 at OTDM mode.

## Audio ADC/DAC

**Address= 8'hF0**

Audio ADC/DAC Test Mode							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
	ADAC_mute	ADAC_r eset	ADAC_p d		AADC_t est	AADC_r eset	

**AADC\_reset:** Audio ADC reset. (R/W: Active high)

**AADC\_test:** Audio ADC test pin.

**ADAC\_pd:** Audio DAC power down. (R/W: Active high)

**ADAC\_reset:** Audio DAC reset. (R/W: Active high)

**ADAC\_mute:** Audio DAC mute. (R/W: Active high)

**Address= 8'hF1**

Audio DAGC Config 1							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
<b>4'h8</b>				<b>4'h8</b>			
<b>AADC_DAGC_2</b>				<b>AADC_DAGC_1</b>			

**AADC\_DAGC\_1:** Audio ADC 1 digital gain control.

**AADC\_DAGC\_2:** Audio ADC 2 digital gain control.

ADAC_DAGC_X[3:0], MIXGAIN_X[3:0]					
Set	Real Gain	dB	Set	Real Gain	dB
4'h0	0	-	4'h8	1.00	0
4'h1	0.125	-18.06	4'h9	1.25	1.94
4'h2	0.25	-12.04	4'hA	1.5	3.52
4'h3	0.375	-8.52	4'hB	1.75	4.86
4'h4	0.5	-6.02	4'hC	2.00	6.02
4'h5	0.625	-4.08	4'hD	2.25	7.04
4'h6	0.75	-2.50	4'hE	2.50	7.96
4'h7	0.875	-1.16	4'hF	2.75	8.79

**Address= 8'hF2**

Audio DAGC Configuration 2							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
4'h8				4'h8			
AADC_DAGC_4				AADC_DAGC_3			

**AADC\_DAGC\_3:** Audio ADC 3 digital gain control.

**AADC\_DAGC\_4:** Audio ADC 4 digital gain control.

**Address= 8'hF3**

Audio DAGC Configuration 3							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
4'h8				4'h8			
AADC_DAGC_P				AADC_DAGC_5			

**AADC\_DAGC\_5:** Audio ADC 5 digital gain control.

**AADC\_DAGC\_P:** Audio ADC digital gain control, source is selected from REGF8:  
ADAC\_SRC .

**Address= 8'hF4**

Audio ADC Format							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	2'h0		0	0
			AADC_MULCH	AADC_FSRATE	AADC_I2SMODE		

**AADC\_I2SMODE:** (Digital I2S/DSP record interface): (master only)

1'b0: I2S mode

1'b1: DSP mode

**AADC\_FSRATE:** (Digital I2S/DSP record interface)

2'b00: 48KHz

2'b01: 24KHz

2'b10: 16KHz

2'b11: 8KHz

**AADC\_MULCH:** When 1, out 5 channels in record path.

When 0, out 2 channels in record path.

**Address= 8'hF5**

MIX Gain Configuration 1							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
4'h2				4'h2			
MIXGAIN_2				MIXGAIN_1			

**MIXOUT =**

$$\begin{aligned}
 & \text{AIN1} * \text{ADC_DAGC\_1} * \text{MIXGAIN\_1} + \text{AIN2} * \text{ADC_DAGC\_2} * \text{MIXGAIN\_2} + \\
 & \text{AIN3} * \text{ADC_DAGC\_3} * \text{MIXGAIN\_3} + \text{AIN4} * \text{ADC_DAGC\_4} * \text{MIXGAIN\_4} + \\
 & \text{AIN5} * \text{ADC_DAGC\_5} * \text{MIXGAIN\_5} + \text{ADATP} * \text{MIXGAIN\_P}
 \end{aligned}$$

**Address= 8'hF6**

MIX Gain Configuration 2							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
4'h2				4'h2			
MIXGAIN_4				MIXGAIN_3			

Refer to REG F5

**Address= 8'hF7**

MIX Gain Configuration 3							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
4'h2				4'h2			
MIXGAIN_P				MIXGAIN_5			

Refer to REG F5

**Address= 8'hF8**

Audio DAC Format							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	3'h0			0	0	0	0
ADAC_T IME	ADAC_SRC			ADAC_FSRATE	ADAC_I 2SMOD E	ADAC_P RCH	

**ADAC\_PRCH:** When ADAC selecting the playback input source and PLAY\_PRCH=0, ADAC chooses the playback left channel. Otherwise use playback right channel.

**ADAC\_I2SMODE:** (Digital I2S/DSP playback interface): (mater only).

1'b0: I2S mode

1'b1: DSP mode.

**ADAC\_FSRATE:** (Digital I2S/DSP playback interface):

2'b00: 48KHz

2'b01: 24KHz

2'b10: 16KHz

2'b11: 8KHz

**DAC\_SRC:**

3'h0: ADATP (playback)

3'h1: MIXOUT

3'h2: AIN\_1

3'h3: AIN\_2

3'h4: AIN\_3

3'h5: AIN\_4

3'h6: AIN\_5

**ADAC\_TIME:**

When 1, use ADAC\_FSRATE, ADAC mode to generate ACLKP/ASYNP.

Otherwise share the same timing signals with ACLKR/ASYNR.

**Address= 8'hF9**

Audio ADC/DAC Test Mode							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
			AADC_p d5	AADC_p d4	AADC_p d3	AADC_p d2	AADC_p d1

**AADC\_pdX:** Power down of Audio ADC X, active high.

**Address= 8'hFA**

Audio ADC/DAC Bias							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
4'hA				4'hA			
ADAC_bias				AADC_bias			

**ADAC\_bias:** Audio DAC's bias setting.

**AADC\_bias:** Audio ADC's bias setting.

**Address= 8'hFB**

Audio ADC/DAC Test Mode							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
3'h0			0	0	0	2'h0	
AADCSEL			SW_AU DIOTST EN			VADCBYPOPT	

**VADCBYPOPT:**Video ADC bypass source option

2'b00: external A/B channel mode.

2'b01: external only A channel mode.

2'b10: external ADI mode.

**SW\_AUDIOTSTEN:**When 1, chip enter to Audio Test mode, and drives Audio ADC/DAC test signal to I/O pins.

**AADCSEL:** Under Audio ADC test mode.

3'h0: AADC\_1[15:0] selected to output pins.

3'h1: AADC\_2[15:0] selected to output pins.

3'h2: AADC\_3[15:0] selected to output pins.

3'h3: AADC\_4[15:0] selected to output pins.

3'h4: AADC\_5[15:0] selected to output pins.

**Address= 8'hFC**

Audio Cascade Mode Control							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
2'h0	0	0	0	0	0	0	0
casID	SWCAS LVL0	SWCASI D	MIXCAS EN	I2SRCA SEN	ACASIE N	ACASO EN	

**casID** and **SWCASLVL0** are effective only if (**SWCASID=1**). In this case SW should program these two registers to indicate the cascade ID of current stage. Please refer to the table below. If (**SWCASID=0**), these two registers are “don’t care”.

ID of Current Stage	<b>SWCASLVL0</b>	<b>casID[1:0]</b>
0	1'b1	2'b00
1	1'b0	2'b00
2	1'b0	2'b01
3	1'b0	2'b10

**SWCASID:** 0: The cascade ID is determined by HW logic.

1: The cascade ID is determined by SW through registers **casID** & **SWCASLVL0**.

**MIXCASEN:** When set as 1 the analog audio input AIN5 will be included in the cascade operation (using ADATM).

**I2SRCASEN:** 0: Audio cascade operation is disabled.

1: Audio cascade operation is enabled.

**ACASIEN:** 0: Cascade input pin (ALINKI) is disabled.

1: Cascade input pin (ALINKI) is enabled.

**ACASOEN:** Output enable control of cascade output pin (ALINKO). Active High.

**Address= 8'hFD**

Audio Cascade Mode Control and Status							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
1	0	0	0	0	0	$2'h0$	
FCLK14 4	I2SDAT AWIDTH		ACASID CHG	ACASA CT	ACASID VLD	ACASID	

**FCLK144:** Set as 0 when PLL is configured to output 108 MHz clock.

Set as 1 when PLL is configured to output 144 MHz clock.

**I2SDATAWIDTH:** 0: The I2S/DSP interface uses 16-bit data.

1: The I2S/DSP interface uses 8-bit data.

**ACASIDCHG:** (RO, Write One to Clear)

This flag is asserted when a change in **ACASID** is detected.

**ACASACT:** (RO)

This flag is asserted when audio cascade is in operation.

**ACASIDVLD:** (RO)

0: The value of the register **ACASID** is not valid.

1: The value of the register **ACASID** is valid.

**ACASID:** (RO) Indicate the cascade ID recognized by HW.

0: The ID of current stage is 1 or 0.

1: The ID of current stage is 2.

2: The ID of current stage is 3.

**Address= 8'hFE**

Mixed Audio Cascade & Audio Record 2							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
ADATM OPT						ADATR_2EN	

**ADATMOPT:** Set this bit the same value as **MIXCASEN**.

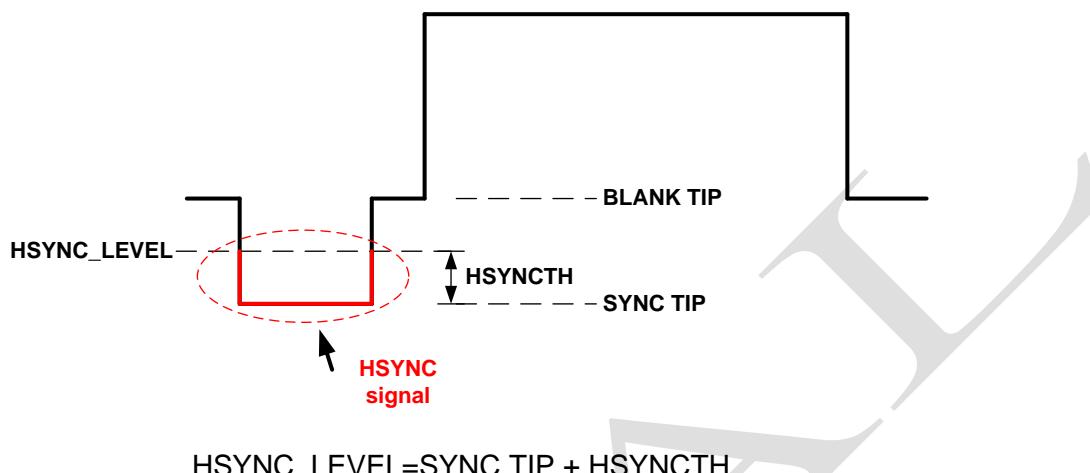
**ADATR\_2EN:** Set as 1 to enable audio record channel 2 (using MI2CD1)

**Address= 8'hFF**

REVNUM							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h65							
REVNUM							

## Video Decoder

**Hsync signal:**



**Address= 8'h00**

VD Control							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	1	0	1	0
BBRSTZ	IFLDFA STSW	FASTS WEN	S_Video	ADC_A	ADI_AD C	EN	SRSTZ

**SRSTZ:** SW reset video decoder, WO

**EN:** Enable Video decoding function

**S\_Video:** input signal is S-Video

**FASTSWEN:** Enable fast switch function

**IFLDFASTSW:** Set 1 : Fast switch boundary at every field end. Only Valid when REG04[3] : 1'b0.

Set 0: Fast switch boundary at frame end.

**BBRSTZ:** BB reset only, WO

**Address= 8'h01**

WATCHSEL							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
4'hf				0	0	2'b01	
AGC_LMT							

**AGC\_LMT:** Analog AGC range

## AGC

**Address= 8'h02**

AGC							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
4'h0				1	0	1	1
AGC_gain			RESERV ED	AGC_DT RACKEN	HWAGC EN	SYNCC AGCEN	

**SYNCCAGCEN:** Set 1, enable CAGC gain update.

**HWAGCEN:** Hardware AGC enable

**AGC\_DTRACKEN:** Dynamic sync tip tracking enable

**AGC\_gain:** SW set AGC gain, RW

**Address= 8'h03**

AGCDOWN_TH							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h63							
AGCDOWNTH[7:0]							

**AGCDOWNTH:** ADC couldn't larger than 867, if it is, will decrease the agc\_gain.

**Address= 8'h04**

AGCDOWN_TH							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	2'h3	
<b>FASTSWOPT</b>				<b>OFASTSW</b>		<b>AGCDOWNTH[9:8]</b>	

**OFASTSW:** Set 1: FASTSW control from input PIN(MPOUT).

Set 0: FASTSW source from internal logic related to FASTSWOPT, RW

**FASTSWOPT:** Set fast switch frame length ((FASTSWOPT+1)x8), RW

## Video Detection Misc

**Address= 8'h05**

HSYNCTH							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h30							
HSYNCTH							

**HSYNCTH:** Set horizontal sync threshold level

**Address= 8'h06**

Vdet_misC							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	1	0	1	1
<b>MONOUT</b>	<b>MUKSEL</b>			<b>BLACKOUT</b>	<b>SETUP_7.5IRE</b>	<b>OCCIREN</b>	<b>ColorPOUT</b>

**ColorPOUT:** Set 1, VD will drive Color panel when no video signal detected, otherwise drive black panel. Color panel setting see 0x2A[6:4]

**OCCIREN:** Set 1, VD will out CCIR656

**SETUP\_7.5IRE:** Set 1, add 7.5 IRE to the BLANK\_TIP

**BLACKOUT:** Set 1, VD will drive black panel or blue panel when no video signal detected.

**MONOUT:** force CCIR656 Cb=128, Cr=128

### Color Killer

**Address= 8'h08**

ColorKill TH							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h20							
CBDIFFTH[7:0]							

**CBDIFFTH:** Set the color burst difference threshold

### 2D Comb Filter

**Address= 8'h09**

Com2D_CFG							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
			FORCE_MONO		FORCE_VCOMB	NOTCHFLTSEL	DIS_VCOMB

**DIS\_VCOMB:** Set 1 to disable vertical comb filter

**NOTCHFLTSEL:** Set 0, use the wide band notchfilter

Set 1, use the narrow band notchfilter

**FORCE\_MONO:** Set 1 to force the MONO signal mode.

**Address= 8'h0C**

PAL SW CFG							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
2'h0	5'h1						0
Y_SHARP_GAIN	RESERVED						PALSW OPT

**PALSWOPT:** Set 1 to use standard pal switch define to demodulation.

For line lock camera, set this bit to 1.

**Y\_SHARP\_GAIN:**

2'h0 : no sharpness function

2'h1: sharpness gain 0.5

2'h2: sharpness gain 1

2'h3: sharpness gain 2

**Address= 8'h10**

VD Decoder status							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
PAL_Nc	PAL-I,B,B1,G,H,D/ PAL_N	PAL_M	PAL_60	NTSC-443	NTSC-J/NTSC-M	COLOR KILL_525	COLOR KILL_625

The register show the video decoded status

**RO.** Set 1 to enable SW force mode.

**Address= 8'h11**

VD_STS							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
CLKLO CK_STS T							DET_NO NILT

**DET\_NONILT:** RO. Detect the non-interlaced signal format.

**CLKLOCK\_STST:** RO. Clock offset lock status

**Address= 8'h12**

DAGC_LMT							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
4'h3				4'hf			
CLKOFF_LOCK				DAGC_LMT			

**DAGC\_LMT:** Digital AGC range

**CLKOFF\_LOCK:** Clock offset locking function. 4'h0: always tracking

Others: clock offset lock within CLKOFF\_LOCK \* 8 ppm.

**Address= 8'h13**

VD_CFG							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	1	1	0	1	0	1	1
SWFAR 54MD	HWFAR 54OPT	GAINLO CK_OPT	CLKOFF DIS	CBADJ	BLANK_ SHIFTE N	ALINEL OCK	CLKOFF _TRACK EN

**CLKOFF\_TRACKEN:** CLKOFFSET tracking enable

**ALINELOCK:** active line lock option, fixed line start position.

**BLANK\_SHIFTEN:** set 1, blank level will be modified according to color burst mean value per line.

**CBADJ:** Color burst adjust

**CLKOFFDIS:** Disable clock offset tracking function

**GAINLOCK\_OPT:** Enable gain locking function after 16 frame decoded.

**HWFAR54OPT:** Set 1, FAR4FS will operate in 54Mhz when detecting 4.43 subcarrier

**SWFAR54MD:** Software force FAR4FS operate in 54Mhz.

**Address= 8'h14**

VD_CFG							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	1	0	1	0	1
		LLCFASTMD				VDETOP T	LTRACK OPT

**CLKLOCKOPT:** Set 0 : Always tracking clock offset when

abs(clkoffset)> CLKOFF\_LOCK (REG12[7:4])

Set 1 : keep tracking until first time

abs(clkoffset)< CLKOFF\_LOCK(REG12[7:4])

**LTRACKOPT:** Set 1: Hardware continues active line (video) decoding when miss valid HSYNC signal until video loss.

Set 0: Hardware performs active line (video) decoding until valid HSYNC signal detected.

**VDETOPT:** Set 1: using rising edge of HSYNC signal as line detection timing.

Set0: using falling edge of HSYNC signal as line detection timing.

For long cable application, set this bit to 1.

**LLCFASTMD[1:0]:**

Line lock Auto Detection stable period. Valid when REG3B[5]=1.

Set 0: check line lock mode right after decode started

Set 1: check line lock mode after 8 frames decoded.

Set 2, 3: check line lock mode after 16 frames decoded.

**Address= 8'h15**

CLKOFF_CTL							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	1	1	0	0
				RESERVED	CLKFRA CEN	FIXHSY NC_MDL	SWFIXC LOCKOFF

**SWFIXCLOCKOFF:** Set 1, SW fixed clock offset. Force clock offset value=

{REG25[4:0],REG24[7:0],REG23[7:0]}.

**FIXHSYNC\_MDL:** Set 1, fixed the HSYNC\_LEVEL to be REG05 HSYNCTH.

**CLKFRACEN:** Set 1, enable fraction clock offset tracking.

**Address= 8'h17**

CTI gain							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0				6'd10		
HMIDTR ACK							

**HMIDTRACK:** Set 1: tracking BLANK TIP each line at Front Porch Blanking position (REG4B[7:0]).

Set 0: tracking BLANK TIP at CVBS serration period.

**Note: 6'd10, d=decimal**

**Address= 8'h18**

LOWTRACK							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	1	0
FSHYBC OPT	DISCOL KILL		NONINT EN	CAGCO PT	TRHSYN COPT	LOWTR ACK	TRHSYN CTH

**TRHSYNCTH:** Set 1: enable HW auto update HSYNCTH during video detection.

Set 0: use fix HSYNCTH (REG05[7:0]) during video detection.

**LOWTRACK:** Set 1: tracking SYNC TIP per line(s) from LOWLEVEL TRACKER.

Set 0: tracking SYNC TIP at CVBS serration period.

**TRHSYNCOPT:** Set 1: use fix HSYNCTH (REG05) during video detection

Set 0: enable HW auto update HSYNCTH during video detection.

**CAGCOPT:** Set 1 to enable color AGC.

**NONINTEN:** Set 1 to enable auto detect non-interlaced singal.

**DISCOLKILL:** Set 1 to disable auto detect color kill mode

**FSHYBCOPT:** ONLY valid under FASTSWEN.

Set 1: Keep previous tracked HSYNCTH

Set 0: use REG05 as HSYNCTH

**Address= 8'h20**

AGC gain							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
DAGC Gain				AAGC Gain			

**AAGC Gain:** Analog AGC gain setting, RO

**DAGC Gain:** Digital AGC gain setting, RO

**Address= 8'h21**

SYNC_TIP[7:0]							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0

**SYNC\_TIP:** RO

**Address= 8'h22**

BLANK_TIP[7:0]							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0

**BLANK\_TIP:** RO

**Address= 8'h23**

7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
<b>CLKOFF[7:0]</b>							

**CLKOFF:** RO, internal 2's compliment clock offset tracking status. Unit (ppm)

**Address= 8'h24**

7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
<b>CLKOFF[15:8]</b>							

**CLKOFF:** RO, internal 2's compliment clock offset tracking status. Unit (ppm)

**Address= 8'h25**

7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
<b>SYNC_TIP[20:16]</b>							

**SYNC\_TIP:** RO

**Address= 8'h26**

7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
				BLANK_TIP[9:8]		SYNC_TIP[9:8]	

**BLANK\_TIP:** RO

**SYNC\_TIP:** RO

**Address= 8'h29**

Blue Panel Select							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
						PALBPLP ANL	NTSCBBL PANL

**PALBPLPANL:** Valid when REG06[3]=1. When no signal, SW sets PAL blue panel out.

**NTSCBBLPANL:** Valid when REG06[3]=1. When no signal, SW sets NTSC blue panel out.

When PALBPLPANL=0, NTSCBBLPANL=0. HW takes PAL as default mode.

**Address= 8'h2A**

VD_MISC							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	2'h2	
	ColorOut					MPP_OPT	

**MPP\_OPT:** (Enable when GPOSEL (REG7A[7]) = 1'b1)

2'h0: drive field info to pin.

2'h1: drive Active info to pin.

2'h2: drive NOVID info to pin.

2'h3: drive FASTSW\_SEL info to pin.

VD\_MPP signal pin out:

(VD0,VD1,VD2,VD3)→( MI2CD0, MI2CD1, MI2CD2, MI2CD3)

**ColorOut: valid when REG06[3]=1 and REG06[0]=1.**

3'h0: blue panel

3'h1: red panel

3'h2: white panel

3'h3: green panel

3'h4: magenta panel

3'h7: color rotation mode, blue → red →

white → green → magenta → black → blue...

### Color Process

**Address= 8'h2B**

COLOR_EXT							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	2'h1		0	0	0	1
	CCIRBL ANKOPT	RESERVED				NTSC_C CIREXT	EXT_CO LOR

**EXT\_COLOR:** Set 1, Y/Cb/Cr value from 8'h1~8'hfe

**NTSC\_CCIREXT:** Set 1 in NTSC mode, CCIR656 output 487 active line.

**CCIRBLANKOPT:** Set 1: output blanking period close to standard CCIR656.

Set 0: with short V blank lines before active field start.

**Address= 8'h2C**

Hue							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h0							
Hue[7:0]							

**Hue:** Hue[9:0] = {REG33[1:0],REG2C[7:0]}

10'h0~10'h3ff → 0~360 degree

**Address= 8'h2D**

Saturation							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h10							
Saturation							

**Saturation:** unsigned, Range : 0 ~ 15.9375

8'hff : maximum, about x16 color intensity.

8'h00: (no color)

**Address= 8'h2E**

Contrast							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h80							
Contrast							

**Contrast:** unsigned, Range : 0~2

8'hff: maximum (x2) contrast

8'h80: original signal (x1)

8'h00: minimum contrast

**Address= 8'h2F**

Brightness							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h00							
Brightness							

**Brightness:** signed

8'h7f: brightest

8'h80: darkest

**Address= 8'h30**

INT Mask							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
	MDCHG_1_MAS_K	VLOST_1_MASK	VDET_1_MASK		MDCHG_0_MAS_K	VLOST_0_MASK	VDET_0_MASK

**VDET\_0\_MASK:** Set 1, enable register 0x31 VDET\_0 interrupt function, RW

**VLOST\_0\_MASK:** Set 1, enable register 0x31 VLOST\_0 interrupt function, RW

**MDCHG\_0\_MASK:** Set 1 enable register 0x31 MDCHG\_0 interrupt function, RW

**VDET\_1\_MASK:** Set 1 to enable register 0x31 VDET\_1 interrupt function, RW

**VLOST\_1\_MASK:** Set 1 enable register 0x31 VLOST\_1 interrupt function, RW

**MDCHG\_1\_MASK:** Set 1 enable register 0x31 MDCHG\_1 interrupt function, RW

**Address= 8'h31**

INT status							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
	MDCHG_1	VLOST_1	VDET_1		MDCHG_0	VLOST_0	VDET_0

**VDET\_0:** when detect video signal, the interrupt set, set by HW, set 1 to clear

**VLOST\_0:** when lose video signal, the interrupt set, set by HW, set 1 to clear

**MDCHG\_0:** when detect video signal change, the interrupt set, set by HW, set 1 to clear

**VDET\_1:** valid for fast switch mode channel B, when detect video signal, the interrupt set, set by HW, set 1 to clear

**VLOST\_1:** valid for fast switch mode channel B, when lose video signal, the interrupt set, set by HW, set 1 to clear

**MDCHG\_1:** valid for fast switch mode channel B, when detect video signal change format, the interrupt set, set by HW, set 1 to clear

**Address= 8'h32**

650 Mode							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	1
						S960H	STVL65 0

**S960H :**Sony Effio mode

NTSC mode : 948x480 PAL mode: 936x576

**STVL650:** 960 Mode

When set 1 : NTSC mode 960x480, PAL mode 960x576

When set 0 : NTSC mode 720x480, PAL mode 720x576

**Address= 8'h33**

HUE							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
							Hue[9:8]

**Hue:** Hue[9:0] = {REG33[1:0],REG2C[7:0]}

10'h0~10'h3ff → 0~360 degree

**Address= 8'h34**

FIELD OPTION							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
					FIELD_I NV	FIELD_ ONLY	

**FIELD\_ONLY:** CCIR656 signal output field 0 only

**FILED\_INV:** Inverse output CCIR656 signal field

**Address= 8'h35**

Chroma Average							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	1
						CAVNTS CMD	CAVPAL MD

**CAVNTSCMD:** Set 1, enable NTSC mode Cb/Cr line average.

Set 0, disable.

**CAVPALMD:** Set 1, enable PAL mode Cb/Cr line average.

Set 0, disable.

**Address= 8'h36**

MASK CCIR656 LINE							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
						MASKA LL	PAL_M SK3

**PAL\_MSK3:** Set 1, it will mask field 0 and 1 last lines according to REG37

**MASKALL:** mask all active

**Address= 8'h37**

MASK LINE							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	3'h0			0	3'h0		
	MSK_LINE_F1				MSK_LINE_F0		

**MSK\_LINE\_F0:** When REG36[0] = 1, Mask Field 0 last number of active lines (0-7)

**MSK\_LINE\_F1:** When REG36[0] = 1, Mask Field 1 last number of active lines (0-7)

**Address= 8'h38**

MONO TH							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
1	0	0	5'd31				
MONO_EN				MONO_TH			

**MONO\_TH:** MONO mode AGC threshold. AGC max value 30. when set MONO\_TH 31.

AGC will always less than MONO\_TH.

**MONO\_EN:** Set 0, when no valid color burst detected.

Output CCIR656 Y through Notch filter.

Set 1, when no valid color burst detected. Output CCIR656

Y through Notch filer if AGC\_GAIN>=MONO\_TH, otherwise output

CCIR656 Y with ADC data.

When No valid color burst detected (color kill mode). Output

CCIR656 Cb/Cr with 128 (no color).

**Note: 5'd31, d=decimal**

**Address= 8'h39**

COLOR BURST DETECT							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	3'h4			4'h5			
	COLBSTCYC			COLBsthSEL			

**COLBsthSEL:**Color Burst detection threshold.

4'h0:COLBsth = 0.125\*(BLANK TIP – SYNC TIP)

4'h1:COLBsth = 0.25\*(BLANK TIP – SYNC TIP)

4'h2:COLBsth = 0.375\*(BLANK TIP – SYNC TIP)

4'h3:COLBsth = 0.5\*(BLANK TIP – SYNC TIP)

4'h4:COLBsth = 0.09375\*(BLANK TIP – SYNC TIP)

4'h5:COLBsth = 0.078125\*(BLANK TIP – SYNC TIP)

4'h6:COLBsth = 0.0625\*(BLANK TIP – SYNC TIP)

4'h7:COLBsth = 0.03125\*(BLANK TIP – SYNC TIP)

4'h8:COLBsth = 0

When color burst peak to peak value larger than COLBsthSEL, it's been considered a good color burst signal cycle.

**COLBstCYC:** When COLBstCYC numbers of valid color bust cycle detected, VD will decode video with color and Color AGC will optionally started. Otherwise will enter color kill mode.

**Address= 8'h3A**

CAGC							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
1	0	0	0	0	1	0	0
CAGCE N	CAGCL OCKOP	cagc_gain					

**cagc\_gain:** RO. Chroma gain value. [5:2] integer, [1:0] fractional.

(max 15.75, min 1)

**CAGCLOCKOPT:** Set 1, enable color AGC tracking until CAGC gain stable.

Set 0, color AGC tracking for first 15 video decoded frames.

**CAGCEN :** Set 1, enable color AGC.

**Address= 8'h3B**

Line Lock Camera							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
1	0	0	0	0	0	0	0
CAMLO CKOPT	LOCKC AM_DET	HLOCK DET1	ACTSHIFT				

**ACTSHIFT:** Active region shift, 2's compliment (-16~15)

**HLOCKDET1:** Set 1, to enable auto-detect Line Lock camera.

**LOCKCAM\_DET:** RO, Line lock camera detected. (RO)

**CAMLOCKOPT:** Set 1, when line lock camera used.

**Address= 8'h3C**

LLOCKTH							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h20							
LLOCKTH							

**LLOCKTH:** Line Lock auto detection threshold, valid only when 0x3B[5]=1.

When REG13[1]=1, line boundary difference within a field larger than LLOCKTH, Line Lock Camera detected.

Note: when clock offset tracking unstable and REG13[1]=1, line boundary difference might be large wthin a field.

**Address= 8'h3D**

VD_CFG							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
	ORSTO PT	OBFOV F	OBFUD F	LLFAR4 FSOPT1			LLFAR4 FSOPT

**LLFAR4FSOPT:** Set 1, decode video chroma without clock offset compensation.

Set 0, decode video choma after clock offset compensation.

Set this bit to one for Line Lock Camera.

**LLFAR4FSOPT1:** Set 1, Auto adjust the active region related to clock offset.

When force line lock mode, set this bit to 1;

**OBFUDF:** RO. CCIR output buffer under flow.

**OBFOVF:** RO. CCIR output buffer over flow.

**ORSTOPT:** Set 1, Reset CCIR output buffer when output buffer overflow or underflow.

**Address= 8'h3D**

OUT BUFFER							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h1a							
OBFTH							

**OBFTH:** CCIR656 output buffer ready threshold.

Once CCIR656 output buffer count is larger than

OBFTH, starts output CCIR656 active region.

PS. CCIR656 output buffer max length is 48, set OBFTH around middle level of buffer length.

**Address= 8'h40**

CCIROUT TYP EN							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	0	0	0	0	0	0	0
		H_SAV_ACT	CROPE_N		FLDCHI DEN	EAVCHI DEN	SWCHID EN

**SWCHIDEN:** Valid when REG00[5]=1(FASTSWEN). Add SW channel ID

in first 4 data of active line, valid at fast switch mode.(field/frame)

**EAVCHIDEN:** Valid when REG00[5]=1(FASTSWEN) Add channel ID in EAV[3:0] and SAV[3:0], valid at fasts witch mode. (field/frame)

**FLDCHIDEN:** Valid when REG00[6:5]=2'h3 (**IFLDFASTSW**, FASTSWEN), output CVBS source A to field 0, output CVBS source B to field 1.

**CROOPEN:** Video cropping function enable.

**H\_SAV\_ACT:** Set 1, HSYNC signal will include SAV data, otherwise HSYNC signal only at active region.

**Address= 8'h41**

Cropping Register							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
2'h0		2'h3		2'h0		2'h0	
H_STR[9:8]		H_ACT[9:8]		V_STR[9:8]		V_ACT[9:8]	

**H\_STR[9:8]:** It defined the number of pixels start after SAV.

**H\_ACT[9:8]:** It defined the number of active region.

**V\_STR[9:8]:** It defined VSYNC start after active region line.

**V\_ACT[9:8]:** It defined the number of VSYNC during active region.

H\_STR + H\_ACT < total number of pixels per line.

V\_STR + V\_ACT < total number of lines per field.

**Address= 8'h42**

Cropping Register							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h0							
H_STR[7:0]							

**Address= 8'h43**

Cropping Register							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'hC0							
H_ACT[7:0]							

**Address= 8'h44**

Cropping Register							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h0							
V_STR[7:0]							

**Address= 8'h45**

Cropping Register							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'd240							
V_ACT[7:0]							

Note: 8'd240, d=decimal

**Address= 8'h46**

Cb/Cr Slicer							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
1						3'h2	
SLICER_EN						SLICER_RANGE	

**SLICER\_EN:** CB/CR coring function enable.

**SLICER\_RANGE:** Coring range (0 ~7). When  $128 - \text{SLICER\_RANGE} < (\text{CB/CR}) < 128 + \text{SLICER\_RANGE}$ , force the Chroma value to 128.

**Address= 8'h4B**

BLANK1TIP							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h93							
BLANK1TIP							

**BLANK1TIP:** valid when REG17[7]. Line Blanking sample position.

**Address= 8'h4C**

HSYNCLOWCYC							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
0	7'd20						
	HSYNCLOWCYC						

**HSYNCLOWCYC:** When low level (signal smaller than HSYNC LEVEL) signal exists over HSYNCLOWCYC, it's considered as a HSYNC signal Candidate.

Note: 7'd20, d=decimal

**Address= 8'h4D**

LMARG27							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h30							
LMARG27							

**LMARG27:** Sync singal detect margin after video detect.

**Address= 8'h4E**

MARG27							
7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
8'h30							
MARG27							

**MARG27:** Sync singal detect margin before video detect.

## Electrical Specifications

### Absolute Maximum Ratings Over Operating Free-Air Temperature Range

Supply voltage range	
IOV <sub>DD</sub> to DGND	-0.5V to 4.6V
DV <sub>DD</sub> to DGND	-0.5V to 2.5V
PLL_AV <sub>DD</sub> to PLL_AGND	-0.5V to 2.5V
CH1_AV <sub>DD</sub> to CH1_AGND	-0.5V to 2.5V

Digital input voltage range, V <sub>I</sub> to DGND	-0.5V to 4.6V
Input voltage range, XTAL1 to PLL_GND	-0.5V to 2.5V
Analog input voltage range A <sub>I</sub> to CH1_AGND	-0.2V to 2.0V
Digital Output voltage range, V <sub>O</sub> to DGND	-0.5V to 4.6V
Storage Temperature Range, T <sub>stg</sub>	-65°C to 150°C

### Recommended Operating Conditions

		<b>MIN</b>	<b>TYP</b>	<b>MAX</b>	<b>UNIT</b>
IODV <sub>DD</sub>	Digital I/O supply voltage	2.97	3.3	3.63	V
DV <sub>DD</sub>	Digital supply voltage	1.62	1.8	1.98	V
PLL_AV <sub>DD</sub>	Analog PLL supply voltage	1.62	1.8	1.98	V
CH1_AV <sub>DD</sub>	Analog core supply voltage	1.7	1.8	1.9	V
V <sub>I(P-P)</sub>	Analog input voltage (ac-coupling necessary)	0.25		1.0	V
Audio V <sub>I(P-P)</sub>	Analog input voltage (ac-coupling necessary)		1.5		
V <sub>IH</sub>	Digital input voltage high	2		5	V
V <sub>IL</sub>	Digital input voltage low	-0.3		0.8	V
V <sub>IH_XTAL</sub>	XTAL input voltage high	0.7 PLL_AV <sub>DD</sub>			V
V <sub>IL_XTAL</sub>	XTAL input voltage low			0.3 PLL_AV <sub>DD</sub>	V
I <sub>OH</sub>	High-level output current			2	mA
I <sub>OL</sub>	Low-level output current			-2	mA
I <sub>OH_SCLK</sub>	SCLK high-level output current			4	mA
I <sub>OL_SCLK</sub>	SCLK low-level output current			-4	mA
T <sub>A</sub>	Operating free-air temperature	-40		85	°C

## Crystal Specifications

CRYSTAL SPECIFICATIONS	MIN	NOM	MAX	UNIT
Frequency		27.0/36.0		MHz
Frequency tolerance		±100		ppm

## Electrical Characteristics

$DV_{DD} = 1.8 \text{ V}$ ,  $PLL\_AV_{DD} = 1.8 \text{ V}$ ,  $CH1\_AV_{DD} = 1.8 \text{ V}$ ,  $IOV_{DD} = 3.3 \text{ V}$

For minimum/maximum values:  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ , and for typical values:  $T_A = 25^\circ\text{C}$  unless otherwise noted

## DC Electrical Characteristics

PARAMETER	TEST CONDITIONS (see NOTE 1)	MIN	TYP	MAX	UNIT
$I_{DD(IO_D)}$ Digital I/O supply current	Color bar input		77.3		mA
$I_{DD(D)}$ Digital core supply current	Color bar input		442.4		mA
$I_{DD(PLL_A)}$ Analog PLL supply current			12		
$I_{DD(CH1-A)}$ IDD(A) Analog ADC/DAC supply current	Color bar input		101.1		mA
$P_{TOT}$ Total power dissipation, normal mode	Color bar input		1254.4	205	mW
$P_{DOWN}$ Total power dissipation, power-down mode	Color bar input			15.3	mW
$C_i$ Input capacitance	By design		8		pF
$V_{OH}$ Output voltage high	$I_{OH} = 2 \text{ mA}$	0.8 $IOV_{DD}$			V
$V_{OL}$ Output voltage low	$I_{OL} = -2 \text{ mA}$			0.22 $IOV_{DD}$	V
$V_{OH\_SCLK}$ SCLK output voltage high	$I_{OH} = 4 \text{ mA}$	2.3			V
$V_{OL\_SCLK}$ SCLK output voltage low	$I_{OL} = -2 \text{ mA}$			0.6	V

NOTE 1: Measured with a load of 15 pf.

### Analog Processing and A/D Converters

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$Z_i$ Input impedance, analog video inputs	By design	500			kΩ
$C_i$ Input capacitance, analog video inputs	By design		10		pF
$V_{i(pp)}$ Input voltage range *	$C_{coupling} = 0.1 \mu F$	0.25		1	V
$\Delta G$ Gain control range			12		dB
DNL DC differential non-linearity	A/D only		$\pm 2$		LSB
INL DC integral non-linearity	A/D only		$\pm 3$		LSB
Fr Frequency response	6 MHz		-0.9	-3	dB
SNR Signal-to-noise ratio	6 MHz, 1.0 Vp-p		50		dB
NS Noise spectrum	50% flat field		50		dB
DP Differential phase			1.5		°
DG Differential gain			0.5%		

\* The 0.75-V maximum applies to the sync-chroma amplitude, not sync-white. The recommended termination resistors are 37.4 Ω.

## Timing

### Clocks, Video Data, Sync timing

#### Data Format : CCIR656 output

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
PIXCLK High pulse duration	$t_{hw}$	18.5			ns
PIXCLK Low pulse duration	$t_{lw}$	18.5			ns
CCIR656 data out setup time	$t_{su}$	18.5			ns
CCIR656 data out hold time	$t_h$	18.5			ns

Output:CCIR656

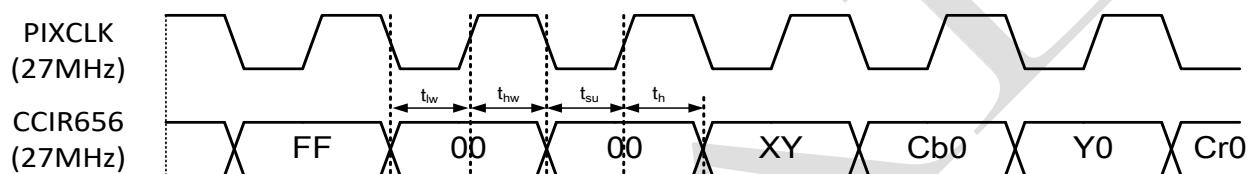


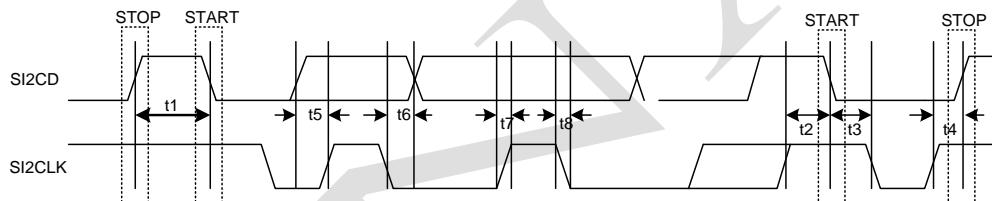
Figure 3-2 . Clocks, CCIR656 Output Data Timing

#### Data Format : CCIR656 input

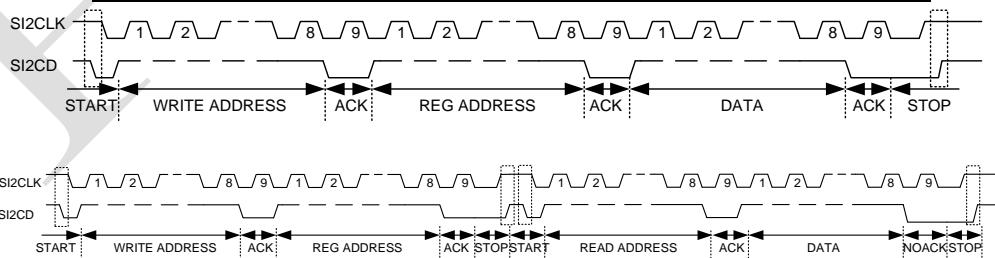
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
PIXCLK High pulse duration	$t_{hw}$	18.5			ns
PIXCLK Low pulse duration	$t_{lw}$	18.5			ns
CCIR656 data out setup time	$t_{su}$	18.5			ns
CCIR656 data out hold time	$t_h$	18.5			ns

### I<sup>2</sup>C Host Port Timing

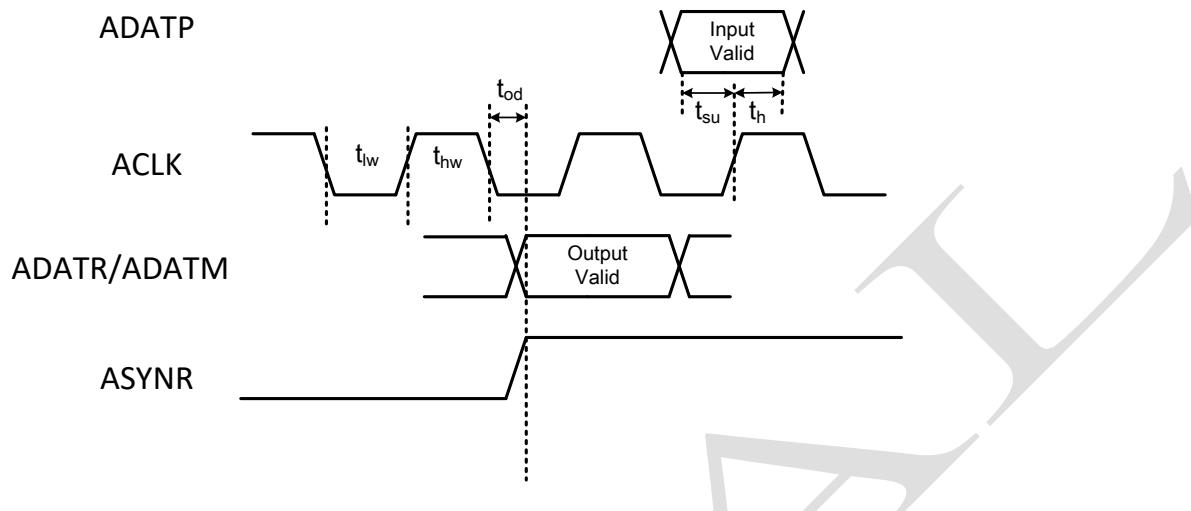
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>1</sub> Bus free time between STOP and START		1.3			μs
t <sub>2</sub> Setup time for a (repeated) START condition		0.6			μs
t <sub>3</sub> Hold time (repeated) START condition		0.6			μs
t <sub>4</sub> Setup time for STOP condition		0.6			μs
t <sub>5</sub> Data setup time		200			ns
t <sub>6</sub> Data hold time		0	50		ns
t <sub>7</sub> Rise time I2CD and I2CLK signal		250			ns
t <sub>8</sub> Fall time I2CD and I2CLK signal		250			ns
C <sub>b</sub> Capacitive load for each bus line			120		pF
f <sub>I2C</sub> I <sup>2</sup> C clock frequency			400		kHz



	Write Address	Read Address
SADD[0] Pull low SADD[1] Pull low	C0	C1
SADD[0] Pull high SADD[1] Pull low	C2	C3
SADD[0] Pull low SADD[1] Pull high	C4	C5
SADD[0] Pull high SADD[1] Pull high	C6	C7

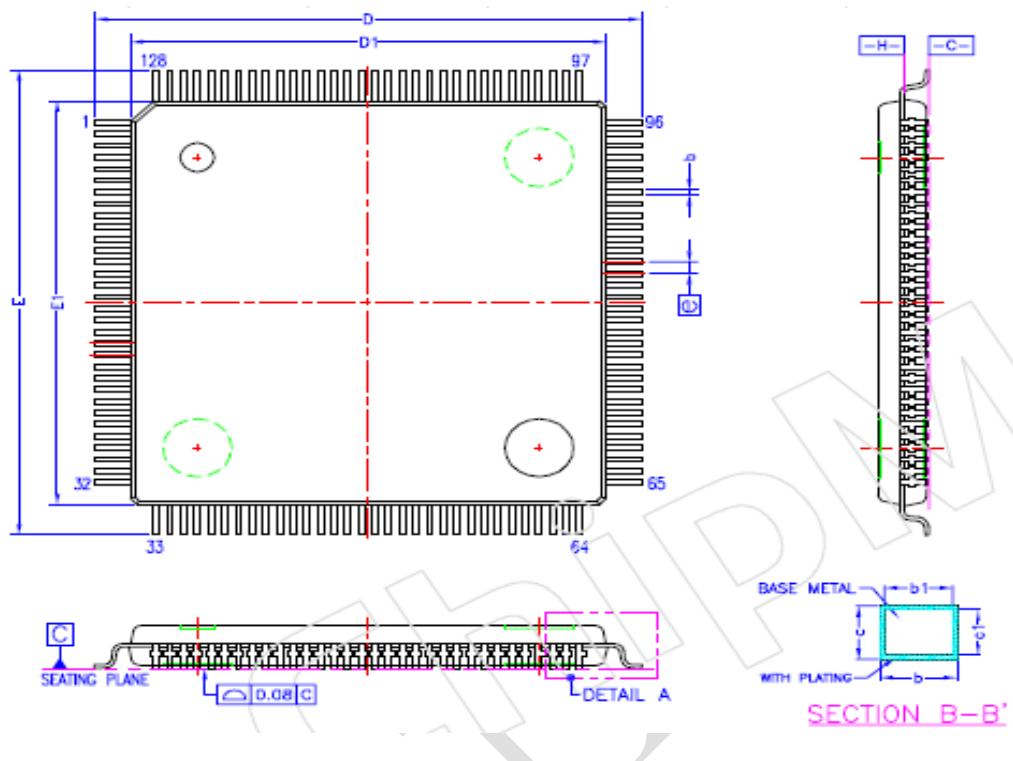


### AC Characteristic of Digital Audio Interface



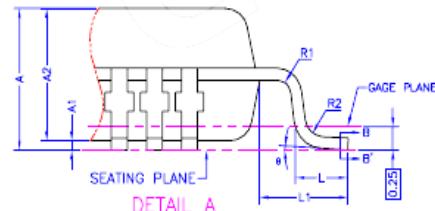
		Min	Typ	Max	Unit
<b>tlw</b>	<b>clock low time</b>				ns
<b>thw</b>	<b>clock high time</b>				ns
<b>tod</b>	<b>output delay time</b>				ns
<b>tsu</b>	<b>input setup time</b>				ns
<b>th</b>	<b>input hold time</b>				ns

## Packaging



SYM.	DIMENSION (MM)			DIMENSION (INCH)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.60	—	—	0.063
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	0.127	0.16	0.004	0.005	0.006
D	15.90	16.00	16.10	0.626	0.630	0.634
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.90	16.00	16.10	0.626	0.630	0.634
E1	13.90	14.00	14.10	0.547	0.551	0.555
G	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.016	0.024	0.030
L1	1.00 REF			0.040 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
g	0"	3.5"	7"	0"	3.5"	7"

- REFER TO JEDEC STD. MS-026
- DIMENSION D AND E ARE DETERMINED AT SEATING PLANE .
- DIMENSION D1 AND E1 ARE DETERMINED AT DATUM .
- DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS WHICH INCLUDE MOLD MISMATCH.
- DIMENSION G DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM B DIMENSION BY MORE THAN 0.08mm.
- ALL DIMENSIONS ARE IN MILLIMETERS.



## Ordering Information

Part Number	Pin Count	Package
DM5866EP	128	LQFP (Pb-Free and Halogen-Free)

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