DAVICOM Semiconductor, Inc.

DM130256

15V / 30V Selectable Output & 258 Hi-V Channels Driver IC

DATA SHEET

Preliminary

Version: DM130256-11-MCO-DS-P01

November 28, 2014

Content

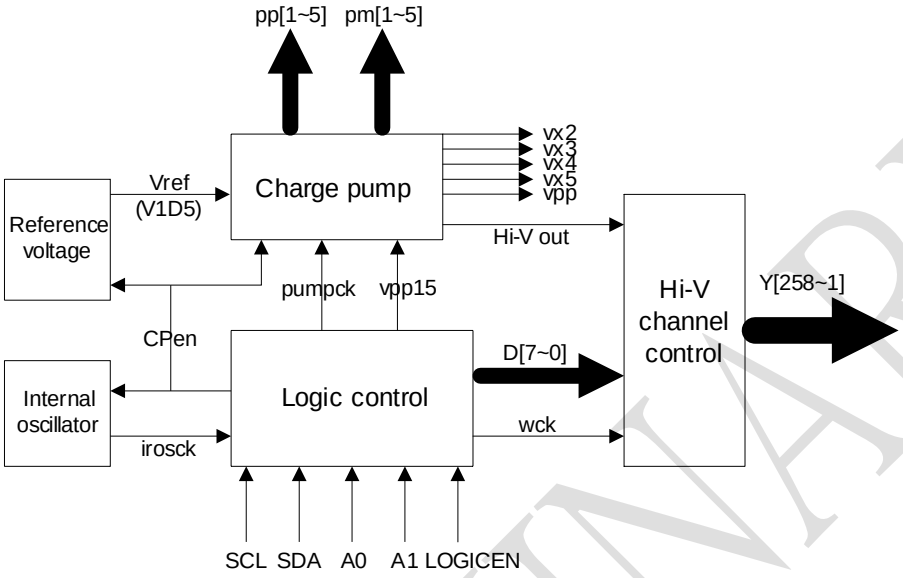
1 General Description

The DM130256 consist of Hi-V charge pump for EPD (Electrophoretic display) application. User can chose 15V or 30V output voltage. All the functions are controlled by 2-wires serial interface or SPI interface. DM30256 support synchronous serial signal control (Maximum support 4 chips).

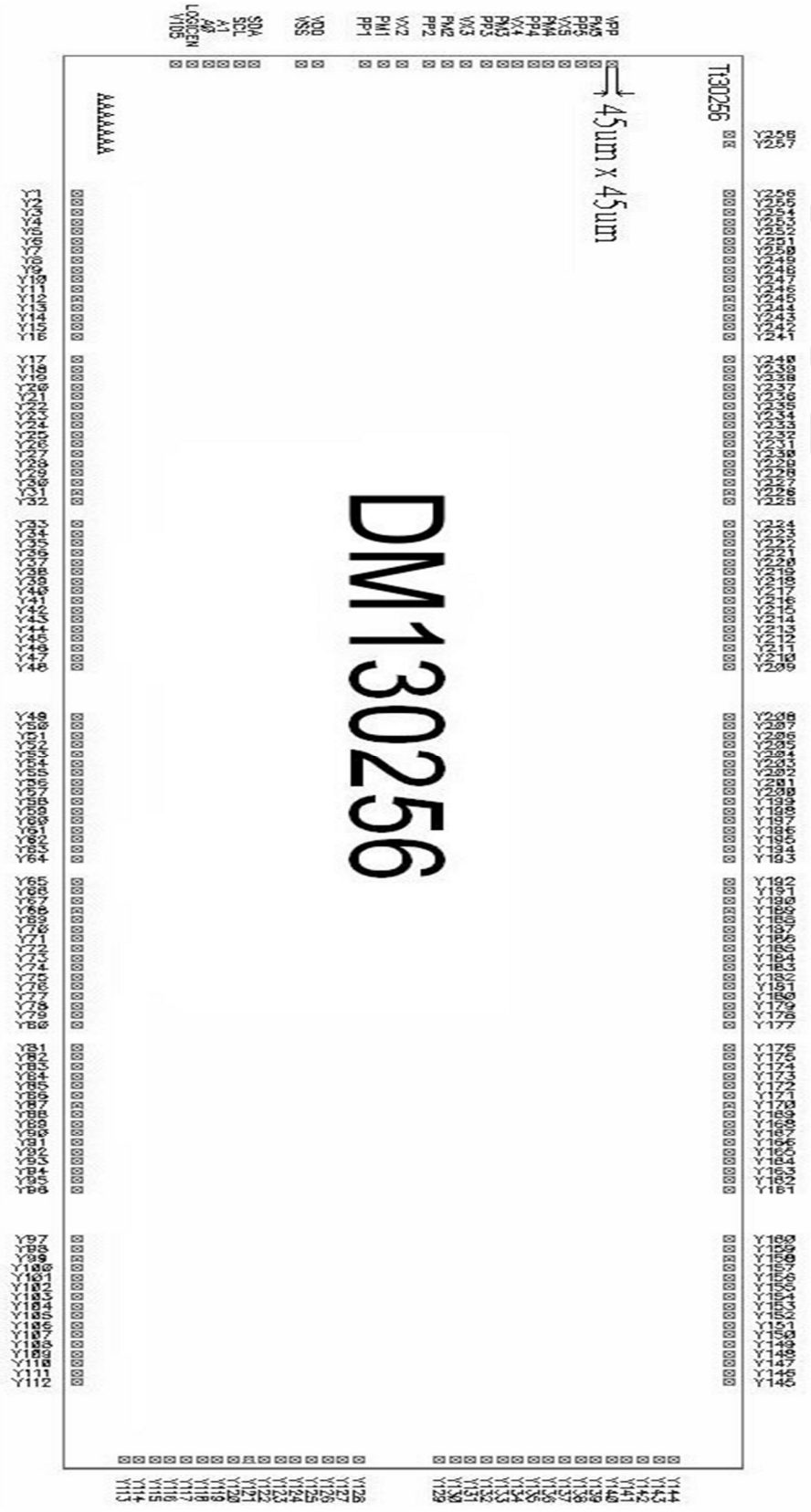
2 Features

- **Selectable 15V or 30V driving voltage for EPD**
- **256 SEG + 1 COM + 1 Background**
- **Charge pump circuit**
- **ON chip RC oscillator**
- **2-wires serial interface**
- **SPI interface control**
- **Voltage regulator**
- **Synchronous serial signal control (Maximum support 4 chip)**

3 Block Diagram



4 PAD Diagram



5 Pin Description

PIN NAME	Description
SCL	2-wires serial interface clock input
SDA / SPIEN	2-wires serial interface data input or SPIEN pin
A1 / SPICK	Device ID setting bit1 or SPICK pin
A0 / SPIDATA	Device ID setting bit0 or SPIDATA pin
LOGICEN	Select the control interface LOGICEN=1 2-wires serial interface LOGICEN=0 SPI interface
VPP	Charge pump output pin about 30v
VPPS	Power source of EPD channels
VX5	Charge pump output pin about 15v
VX4	Charge pump output pin about 7.5v
VX3	Charge pump output pin about 5v
VX2	Charge pump output pin about 2.5v
PP[1:5]	Positive terminal for charge pump capacitor
PM[1:5]	Negative terminal for charge pump capacitor
Y[1:258]	EPD Hi-V channels
VDD	Positive power source
VSS	Negative power source
V1D5	Charge pump reference Voltage

Note: SCL & SDA need pull high resistor 4.7KΩ to VDD

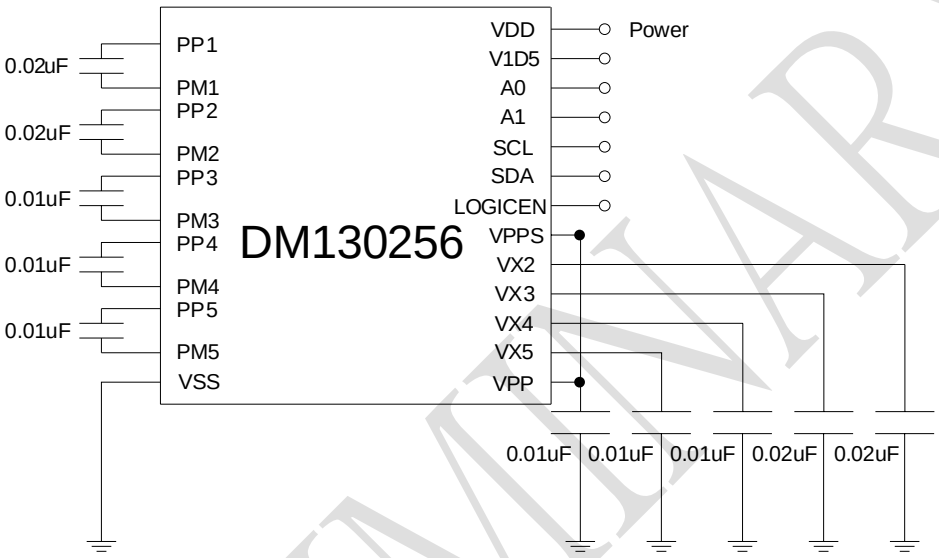
6 Function Description

6.1 Generate Hi-V Driving Bias Supply

6.1.1 Internal Charge Pump Supply

The charge pump circuit can generate Hi-voltage up to 30V. User also can select 0V, 15V or 30V to drive EPD by setting control register.

The value of Hi-voltage that pump can generate as following.
VPP=30V, VX5=15V, VSS=0V



6.1.2 External Driving Bias Supply

External Hi-V power source supply to VPP & VX3. First, user need to turn off internal pump function then supply 30V to VPP, 5V to VX3

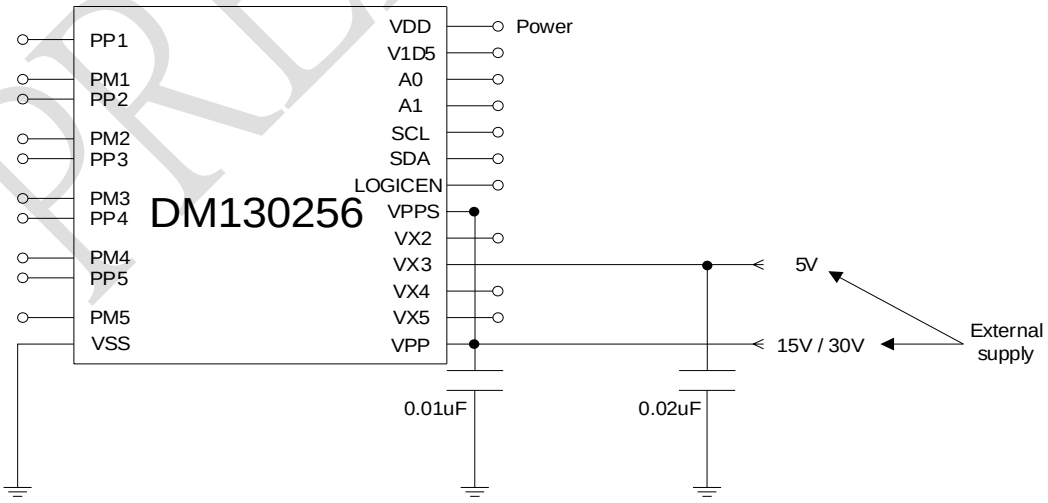
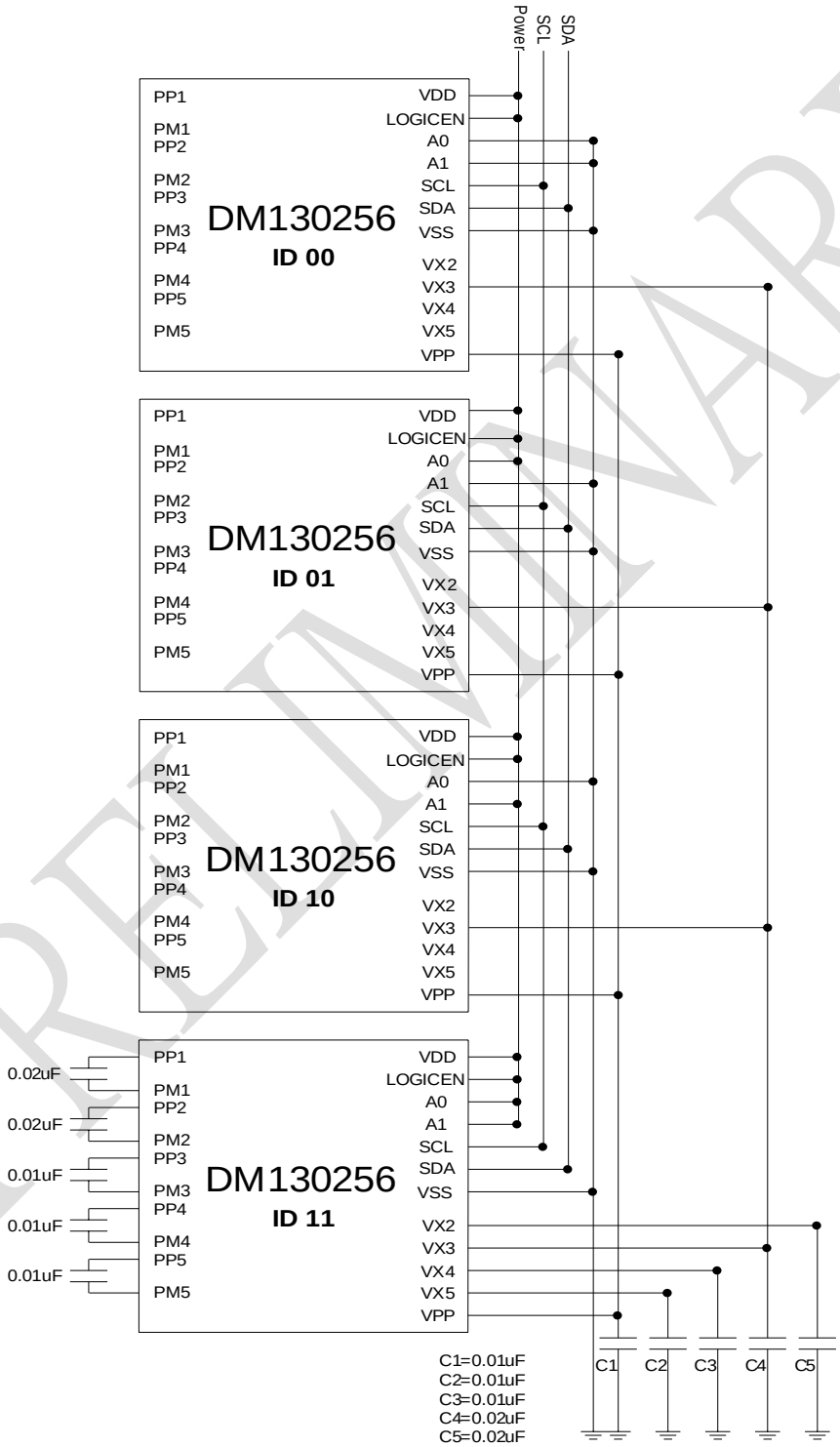


Figure 4

6.2 Multi-drivers Application

With 2-wires serial interface that the host device could control DM130256. (A1,A0) pins correspond the ID setting (Maximum support 4 chips). ID setting see the following figure.

Note: SPI don't support Multi-drivers application.



6.3 EPD Driver Control Register

REGISTER Address	Data							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$00H	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
$01H	Y16	Y15	Y14	Y13	Y12	Y11	Y10	Y9
$02H	Y24	Y23	Y22	Y21	Y20	Y19	Y18	Y17
$03H	Y32	Y31	Y30	Y29	Y28	Y27	Y26	Y25
$04H	Y40	Y39	Y38	Y37	Y36	Y35	Y34	Y33
$05H	Y48	Y47	Y46	Y45	Y44	Y43	Y42	Y41
$06H	Y56	Y55	Y54	Y53	Y52	Y51	Y50	Y49
$07H	Y64	Y63	Y62	Y61	Y60	Y59	Y58	Y57
$08H	Y72	Y71	Y70	Y69	Y68	Y767	Y66	Y65
$09H	Y80	Y79	Y78	Y77	Y76	Y75	Y74	Y73
$0AH	Y88	Y87	Y86	Y85	Y84	Y83	Y82	Y81
$0BH	Y96	Y95	Y94	Y93	Y92	Y91	Y90	Y89
$0CH	Y104	Y103	102	Y101	Y100	Y99	Y98	Y97
$0DH	Y112	Y111	Y110	Y109	Y108	Y107	Y106	Y105
$0EH	Y120	Y119	Y118	Y117	Y116	Y115	Y114	Y113
$0FH	Y128	Y127	Y126	Y125	Y124	Y123	Y122	Y121
$10H	Y136	Y135	Y134	Y133	Y132	Y131	Y130	Y129
$11H	Y144	Y143	Y142	Y141	Y140	Y139	Y138	Y137
$12H	Y152	Y151	Y150	Y149	Y148	Y147	Y146	Y145
$13H	Y160	Y159	Y158	Y157	Y156	Y155	Y154	Y153
$14H	Y168	Y167	Y166	Y165	Y164	Y163	Y162	Y161
$15H	Y176	Y175	Y174	Y173	Y172	Y171	Y170	Y169
$16H	Y184	Y183	Y182	Y181	Y180	Y179	Y178	Y177
$17H	Y192	Y191	Y190	Y189	Y188	Y187	Y186	Y185
$18H	Y200	Y199	Y198	Y197	Y196	Y195	Y194	Y193
$19H	Y208	Y207	Y206	Y205	Y204	Y203	Y202	Y201
$1AH	Y216	Y215	Y214	Y213	Y212	Y211	Y210	Y209
$1BH	Y224	Y223	Y222	Y221	Y220	Y219	Y218	Y217
$1CH	Y232	Y231	Y230	Y229	Y228	Y227	Y226	Y225
$1DH	Y240	Y239	Y238	Y237	Y236	Y235	Y234	Y233
$1EH	Y248	Y247	Y246	Y245	Y244	Y243	Y242	Y241
$1FH	Y256	Y255	Y254	Y253	Y252	Y251	Y250	Y249
$20H	#	#	#	#	#	#	Y258	Y257
$21H	CPEN	C3	VPP15	C2	Load	OEB	VSEL1	VSEL0

Y1~Y258 output setting：
Y1~Y256 mapping to segment pins
Y257 correspond to COM(Common) pin
Y258 correspond to BG(Background) pin

The output voltage (0V,15V,30V) for Y[1~258] are selectable.
If user want Y[1~258] to output 30V or 15V. Setting the correspond bit to “1”
If user want Y[1~258] to output 0V. Setting the correspond bit to “0”

Example：
If users wants Y9, Y11, Y13, Y15 output VPP and Y10, Y12, Y14,Y16 output “0V”
Register $01H = 01010101

Register “$21h” bit7 “CPEN”: Charge pump on / off
CPEN=1 , charge pump enable
CPEN=0 , charge pump disable

Register “$21h” bit6 “C3”： Internal test parameter C3. User has to set up “0” here.

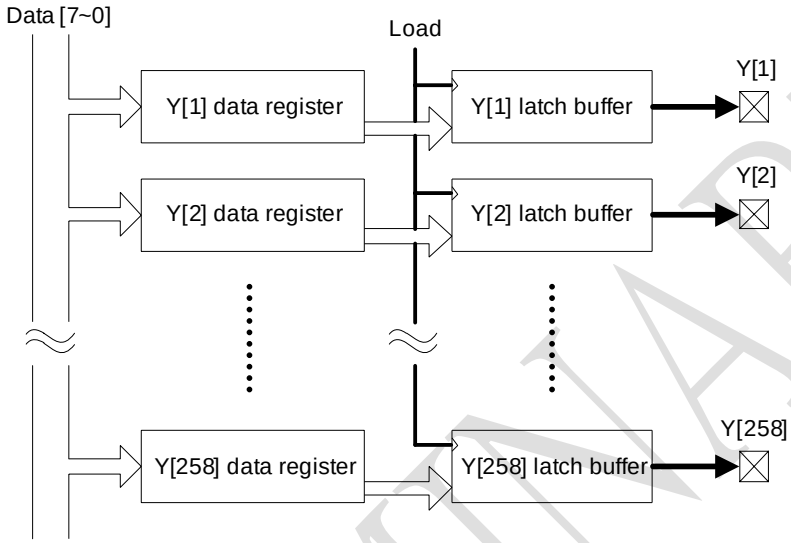
Register “$21h” bit5 “VPP15” ：Half VPP output switch
VPP15=1：Hi-V channels logic high will output VX5, the voltage equal to half VPP.
VPP15=0：Hi-V channels logic high will output VPP.

Register”$21h” bit4 “C2”： Internal test parameter “C2”. Set up “0” here for recommendation.

Register”$21h” bit3 “Load”： Load data from Y[1~258] and then latch out for synchronous
Load=1：Load data from Y[1~258] to output buffer
Load=0：Latch the buffer and output

Output Synchronous

For the reason of output synchronous that user have to set up $21h, bit3 = 1 first. This step will load the data Y[1~258] from register[$00h~$20h] into each buffer. And then set up $21h, bit3 = 0 for the next step. Y [1~258] latch buffers will latch and output the data synchronous.



Note: The data hold time for this bit should be over “1us”. That means, customer set up register $21h.bit3 =1 for latching output then waiting over 1us that will be available for next data.

Register”$21h” bit2 “OEB”： EPD output enable “OEB”. Set up “0” All EPD channels are output available. The “1” setting all channels are high-impedance.

Register”$21h” bit0~1 “VSEL0~1”：Adjustable internal reference voltage
All the selections are shown as blow:

VSEL[1：0]	V1D5
00	1.5V
01	1.6V
10	1.7V
11	1.8V

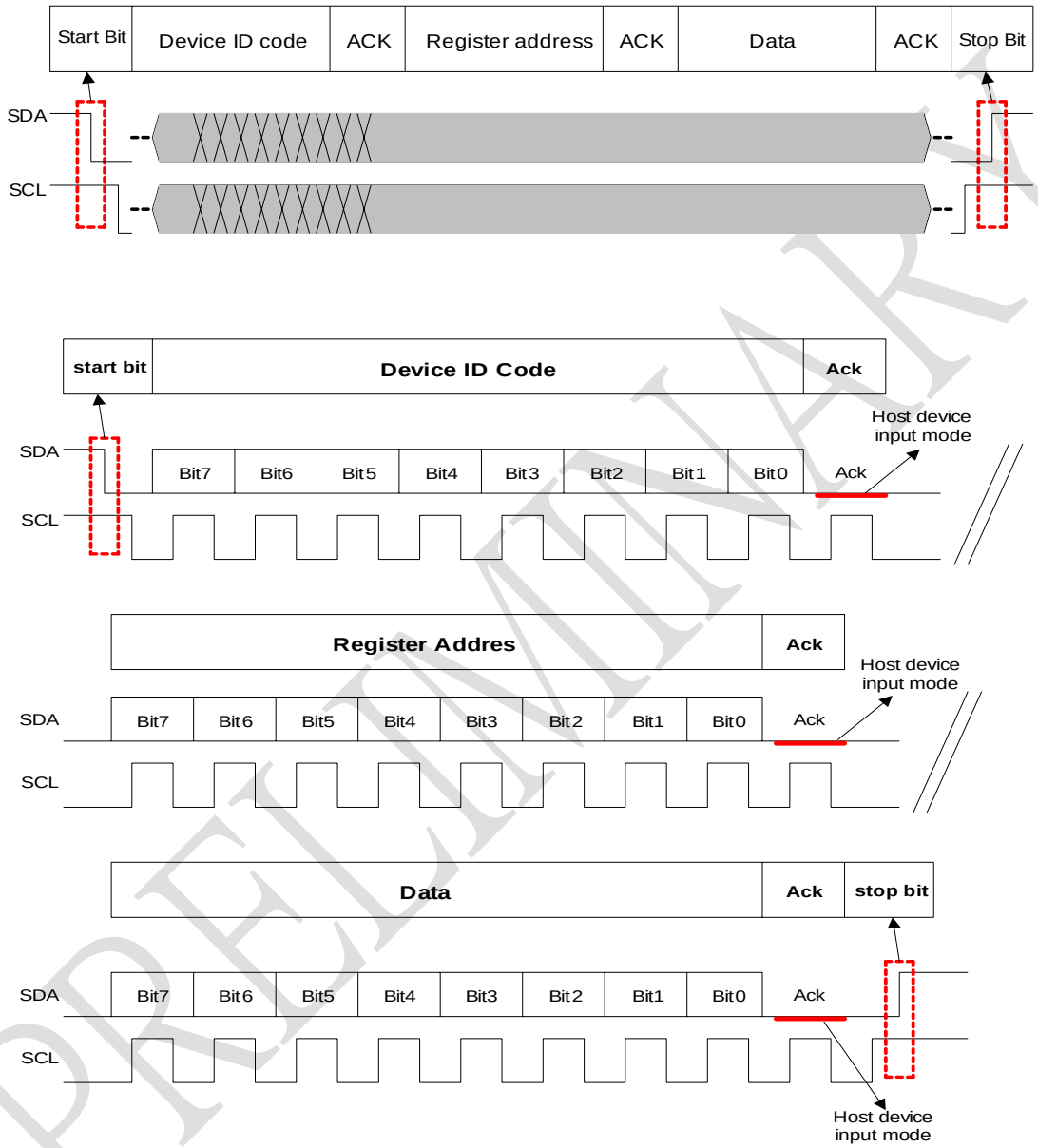
With this setting the VPP voltage could be higher. Because the variation of IC process that we recommend user to adjust V1D5 close to 1.5V therefore VPP will be 30V.

Note:
1. All control registers don’t have initialize value after power on. Users need to initialize all register manual.
2. $xxH means address represent in hexadecimal.
3. “xxxxxxxxb” means 8-bits data of register represent in binary
4. The “VPP” here means the highest pumped voltage, “VX5” means half VPP and “GND” means the most low voltage of system power.
5. Write by default value 00b.

6.4 Control Signal Waveform

6.4.1 Format of One Byte (2-Wires Serial Interface)

This byte could be $00H ~ $21H, see chapter 6.3 EPD driver control register.



Note: Timing diagram above is when SCL=500KHz

Device ID code：
ID code defined by (A0&A1) pins. See figure5 multi-driver application. Control signal input 8-bits “111100A1,A0” (A1,A0)=00,01,10,11 then only matched driver will operate.

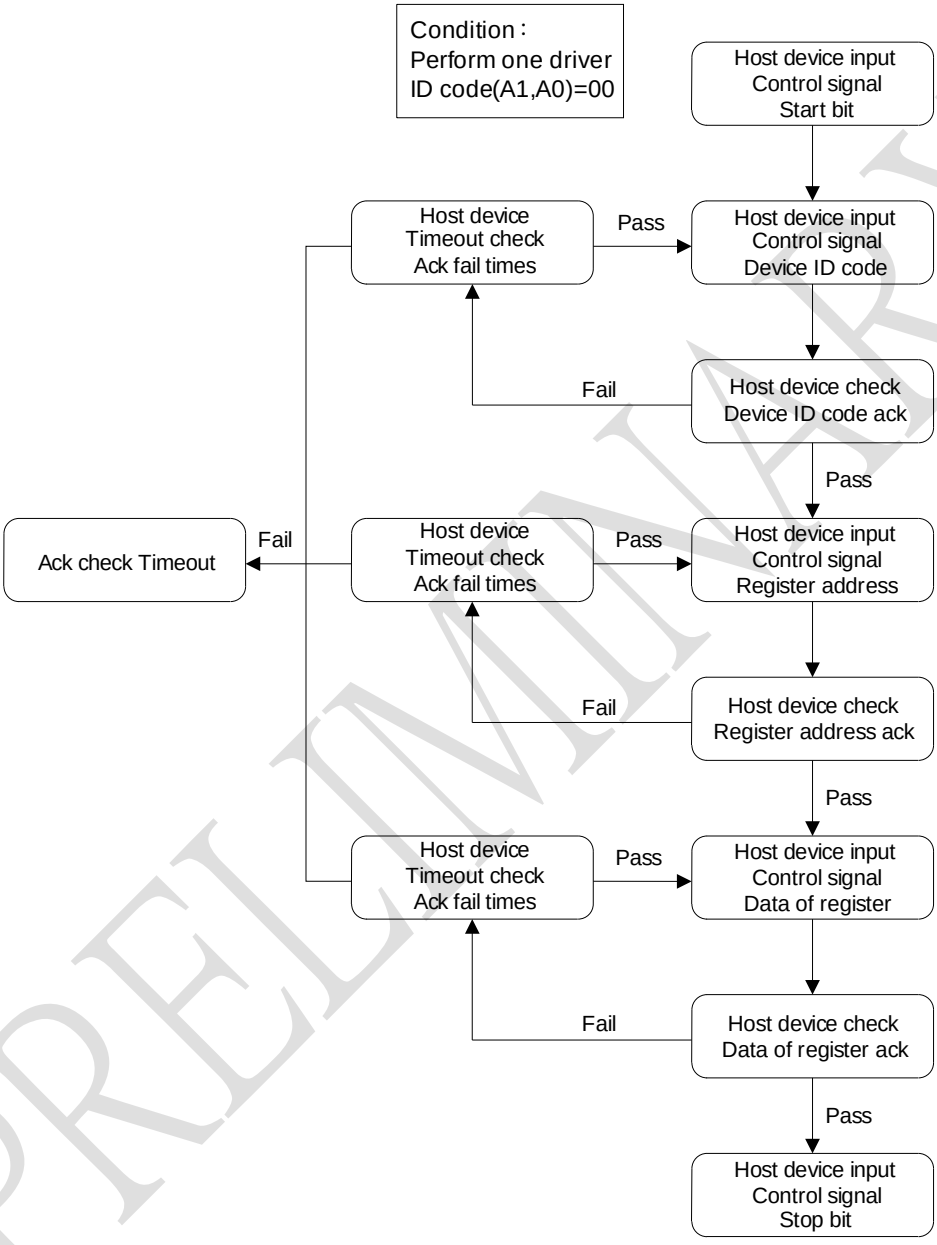
Register address：
Address of control register from $00H ~ $21H. The control signal here follow Device ID code

Data of register：
Definition of all control register see chapter2.3 EPD driver control register.

Condition setting

Perform with one driver and ID code (A1,A0)=00

Operate flow of one byte



Note：

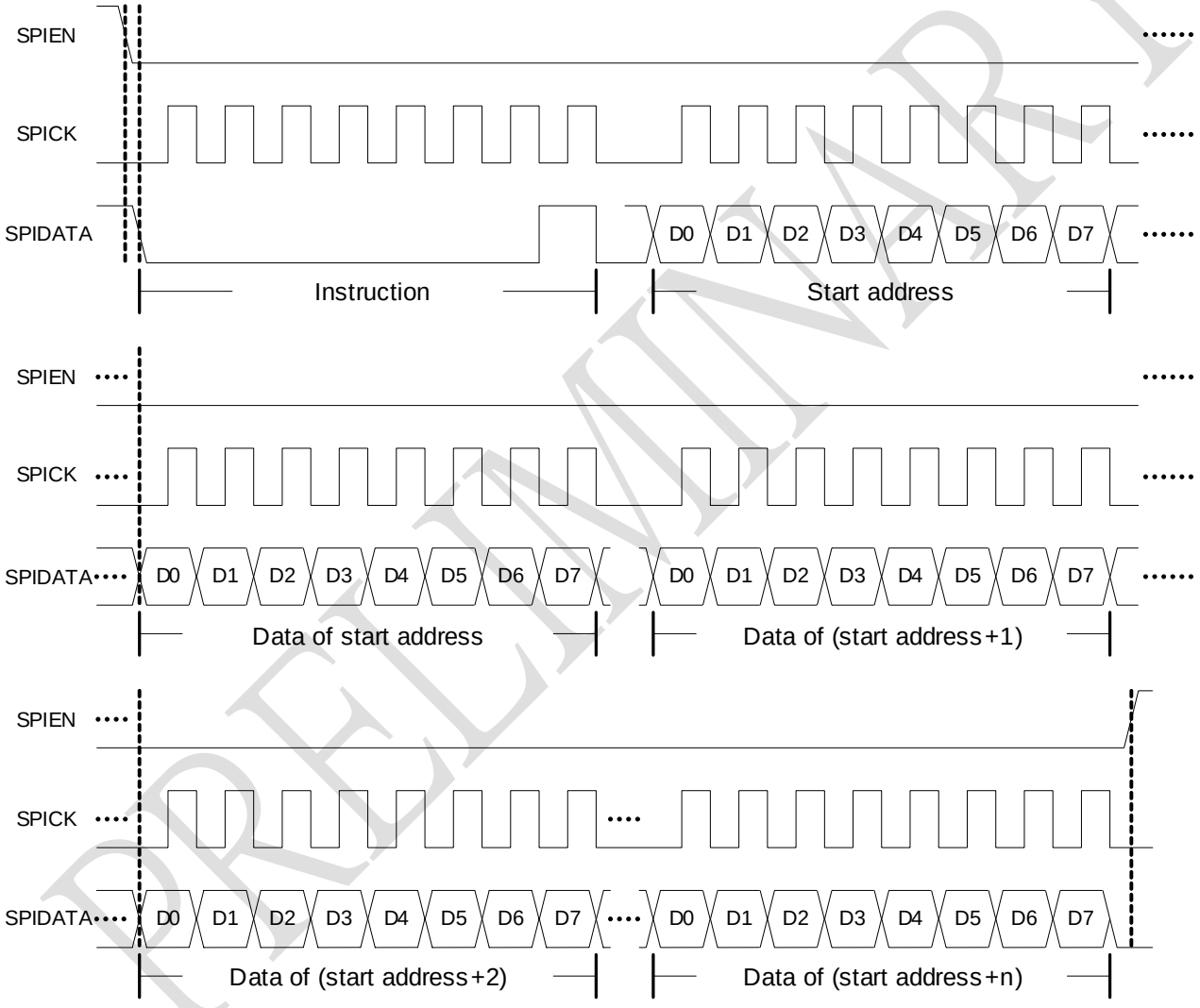
1. According to operating flow above, host device need set SDA to input mode at ACK feedback. Also check ACK feedback “Low” that means current byte transmission pass.
2. Each byte of control register has complete format as figure in P12. Following one-byte format to compose sequent transmission.
3. All the timing of pulse-width in operating flow above represents the minimum acceptable value.
4. Operating flow above is only for reference. For actual situation, please refer to E-paper spec.

6.4.2 SPI Control Waveform

There are two format of controlled signal as below.

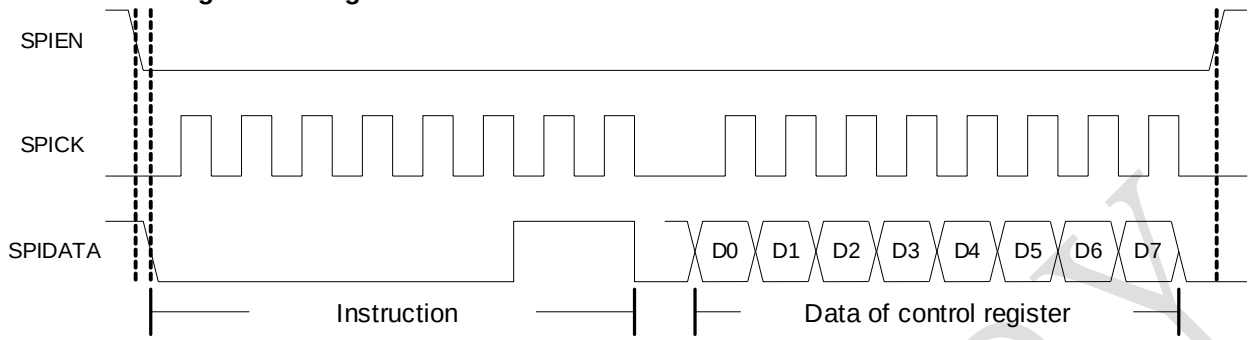
Instruction code	Function
00000001	Writing Data register
00000011	Writing control register

Format of writing data register



1. SPIEN low active
2. SPIDATA input instruction [00000001] for writing data register
3. SPIDATA input start address (selectable from $00H~$0FH)
4. SPIDATA input the data of start address
5. SPIDATA input data of next address. For example, start address from $00H → #FFH(contain of $00H) → #02H (here is the contain of $01H)….etc.
6. SPIEN high disable while data register writing finished.

Format of writing control register

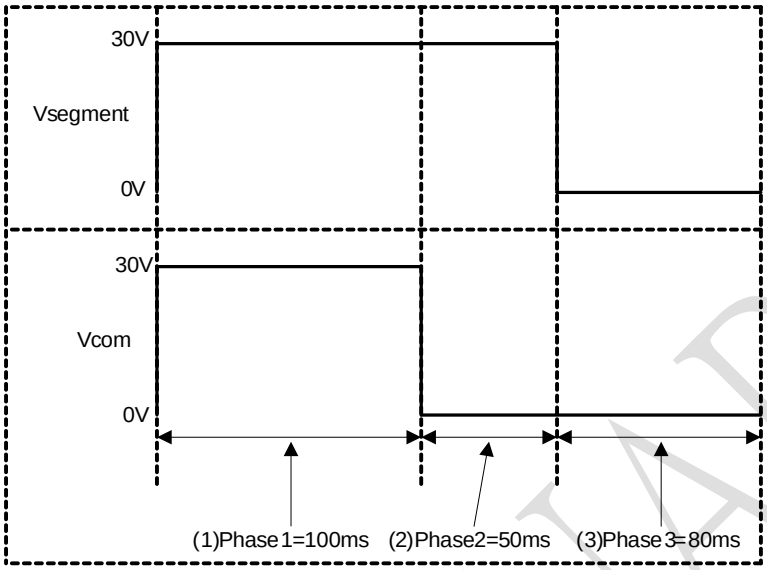


1. SPIEN low active
2. SPIDATA input instruction [00000011] for writing control register
3. SPIDATA input data of control register
4. SPIEN high disable after control register writing done.

Note：

1. ID code setting is not needed in SPI mode.
2. Writing data register could be sequent, but control register is single.

6.4.3 Com & Segment vs. Control Signal



Condition1-1：2-wires serial mode (one driver IC)

VDD=3V, use internal pump function, perform with one driver, pin LOGICEN = 1, ID code (A1,A0)=00
Register $21H. bit5 VPP15=0 , bit6 PUMPH=0 → VPP=30V
Vsegment including Y1~Y256, Vcom = Y257, Vbg = Y258

Condition1-2：SPI mode (one driver IC)

VDD=3V, use internal pump function, perform with one driver, pin LOGICEN = 0
Register $21H. bit5 VPP15=0, bit6 PUMPH=0 → VPP=30V
Vsegment including Y1~Y256, Vcom = Y257, Vbg = Y258

Condition1-1 & 1-2 operate flow

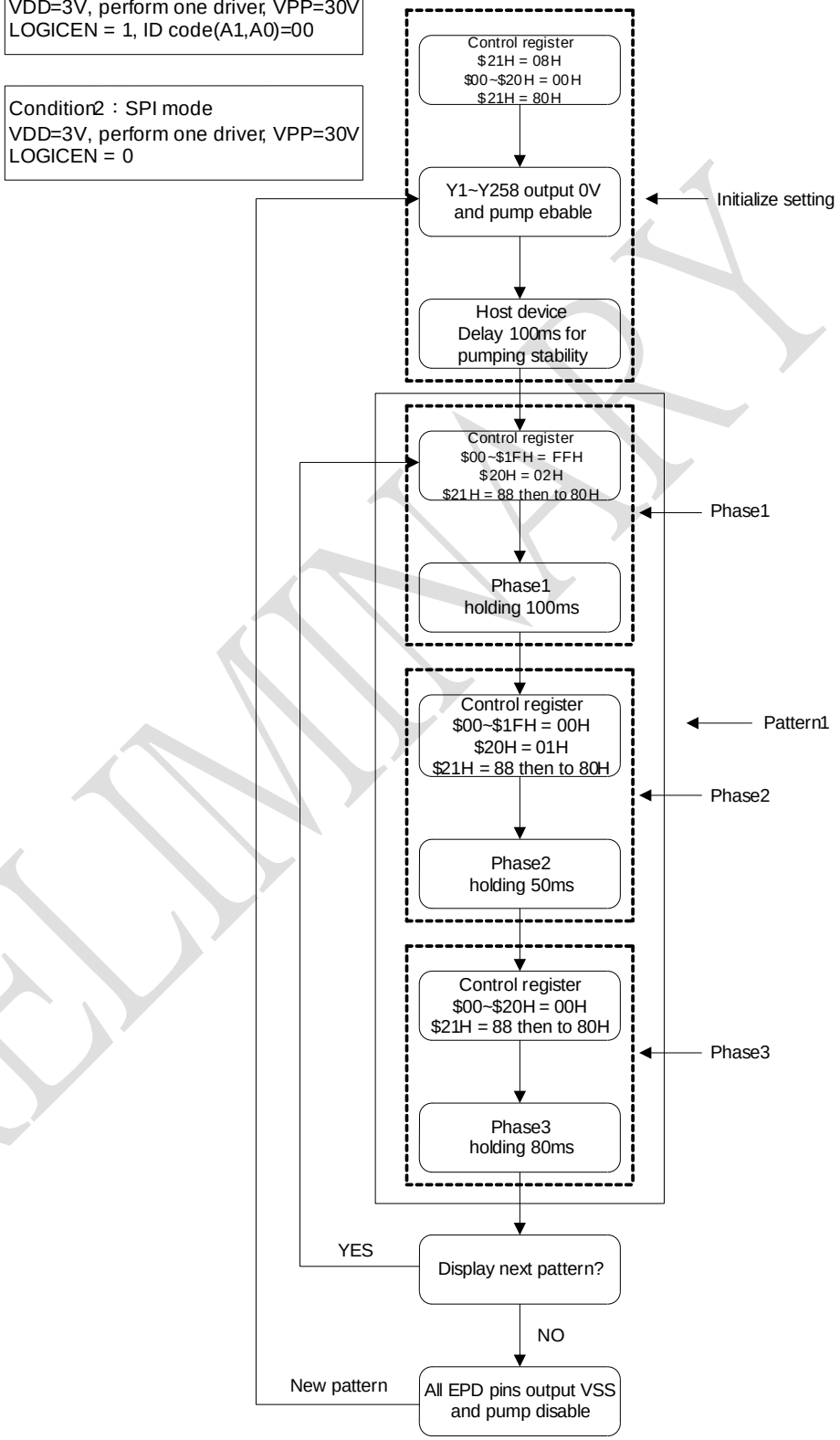
1. Firstly to initial register $21H = “00000000b” to disable pumping. Then $00H~$20H = “00000000b” In this step Y1~Y258 will output “0V”.
   After that $21H = “10001000b” here will latch all EPD pins to “0V” and enable charge pump.
   Note! $21H bit3 load = 1 → 0 will load all data to EPD pins and then latching output state.
2. Host device delay 100ms for internal pumping stability.
3. Controlled register $00H~$1FH = “11111111b” , $20H = “00000010b”
   $21H = “10001000b” then $21H = “10000000b”. Here the display will show up.
   (This setting represent Y1~Y256 & Y258 = 30V and Y257 = 0V)
4. Host device delay 100ms to display at phase1.
5. Controlled register $00H~$01FH = “00000000b” , $20H = “00000001b” , $21H = “10001000b”. Then $21H = “10000000b”. (Y1~Y256 & Y258 output “30V”, Y257 output “0V”).
6. Host device delay 50ms to display at phase2.
7. Controlled register $00H~$20H = “00000000b” , $21H = “10001000b”.
   Then $21H = “10000000b”. (Y1~Y258 output “0V”)
8. Host device delay 80ms to display at phase3.
9. If next pattern is ready to display please keeping $21H = “10000000b”
10. For power saving setting $21H = “00000000b”. The pumping is turning off and Y1~Y258 = “0V” until next display pattern ordered.

Note：

1. After power on the initial step is needed
2. $xxH means address and represent in hexadecimal form.
3. “xxxxxxxxb” means 8-bits data and represent in binary form.
4. Each phase of 1~3 to keep driving voltage for better display contrast.

Condition1：2-wires serial mode
VDD=3V, perform one driver, VPP=30V
LOGICEN = 1, ID code(A1,A0)=00

Condition2：SPI mode
VDD=3V, perform one driver, VPP=30V
LOGICEN = 0



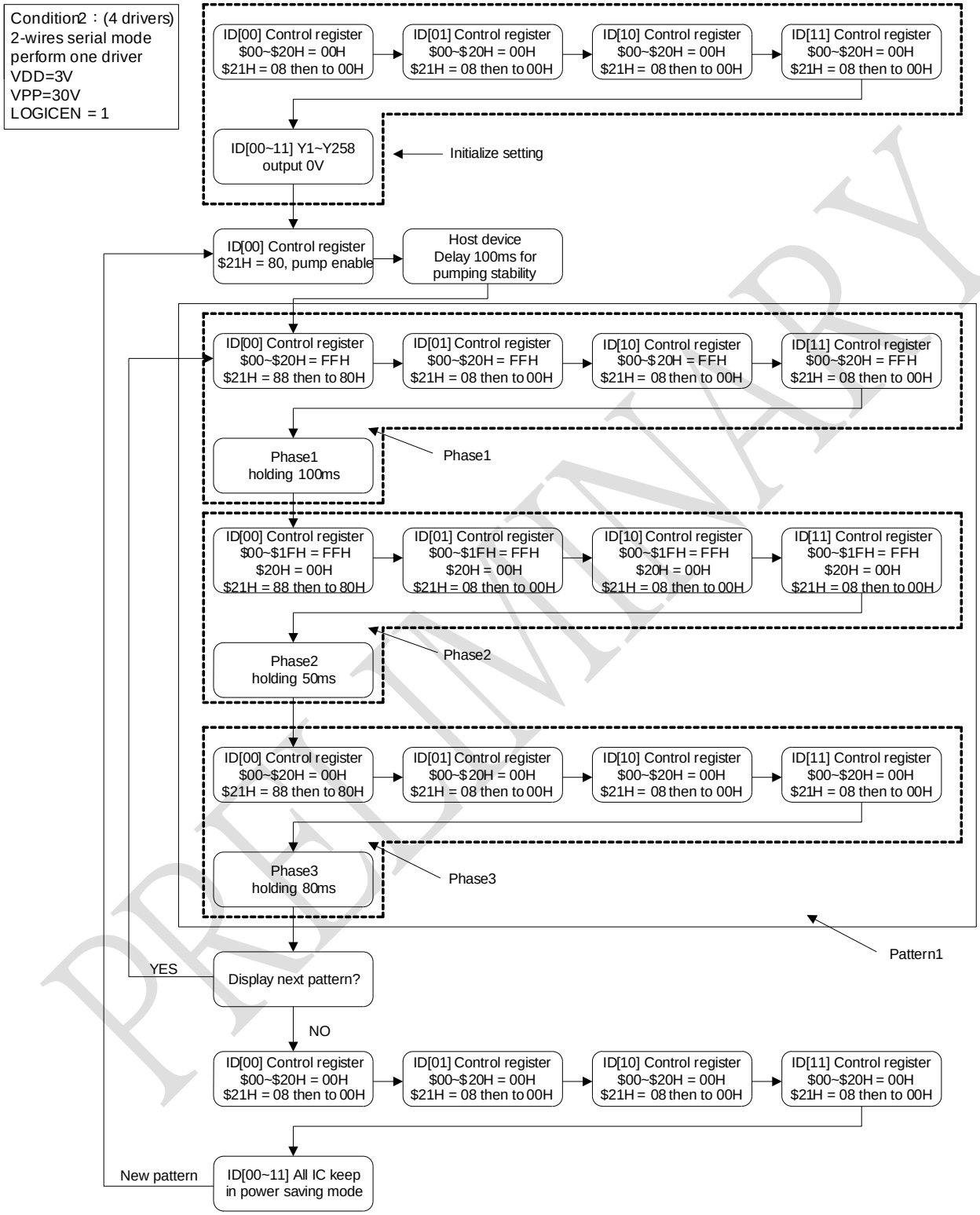
Condition2：2-wires serial mode (cascade four drivers)

VDD=3V , perform with four drivers, one driver be the pumping source and others set up supply from external source, pin LOGICEN = 1
Register $15H. bit5 VPP15=0 , bit6 PUMPH=0 → VPP=30V
Vsegment including Y1~Y256, Vcom = Y257, Vbg = Y258

Condition2 operate flow

1. ID[00] Control register $00H~$20H = “00000000b”, $21H = “00001000b”. This step Y1~Y258 will load data from data register and output “0V” to all EPD pins simultaneously.
   After that $21H = “00000000b” here will latch all EPD pins to “0V”.
   Note! $21H bit3 load = 1 → 0 will load all data to EPD pins and then latch output state.
2. ID[01~11] follow step1 to initialize all EPD pins to output “0V”
3. ID[00] register $21H = “10000000b” to enable charge pump and take ID[00] as pumping source others IC set up supply from external source.
4. Host device delay 100ms for internal pumping stability.
5. ID[00~11] Control register $00H~$20H = “11111111b” , *ID[00] $21H = “10001000b” , ID[01~11] $21H = “00001000b”.Then ID[00] $21H = “10000000b” , ID[01~11] $21H = “00000000b”. Here all EPD pins will output VPP.
6. Host device delay 100ms to display phase1 pattern.
7. ID[00~11] Control register $00H~$1FH = “11111111b” , $20H = “00000000b” , *ID[00] $21H = “10001000b” , ID[01~11] $21H = “00001000b”. Then ID[00] $21H = “10000000b” , ID[01~11] $21H = “00000000b”. All segment and background will output VPP, but Y257 output “0V”.
8. Host device delay 50ms to display phase2 pattern.
9. ID[00~11] Control register $00H~$20H = “00000000b” , *ID[00] $21H = “10001000b” , ID[01~11] $21H = “00001000b”. Then ID[00] $21H = “10000000b” , ID[01~11] $21H = “00000000b”. All EPD pins will output “0V”.
10. Host device delay 80ms to display phase3 pattern.
11. All EPD pins output “0V” and disable pump if there’s no pattern will be display.

Note：$xxH means address and represent in hexadecimal form.
“xxxxxxxxb” means 8-bits data and represent in binary form.



7 Operating Ratings

Description	Symbol	Value			Unit
		Min	Typ	Max	
Working voltage	VDD	2.2	3	3.6	V
Driver supply voltage	Vdrv		30	32	V
Ripple	Vrip		200		mV
Hi-V1	Vpp15		15V	18V	V, (load =15M ohm)
Hi-V2	Vpp30		30V		V, (load =15M ohm)
Stop mode current	Istop		0.1		uA
Pumping enable current	Icpen		350		uA
Input high voltage	VIH		0.8*VDD		V
Input low voltage	VIL		0.2*VDD		V
2wir speed (SCL&SDA)	FI2C			1M	Hz
2wir load capacitance	CI2C		15		pF
SPI speed	FSPI			1M	Hz
SPI load capacitance	CSPI		15		pF

Note：

1. Symbol “2wir” represent SCL & SDA pins
2. Symbol “VPP_{15}” apply to Eink 15V film. For the better life time that customer have to tie each 258 channels to “0V” then turn off charge pumping.

8 Absolute Maximum Ratings

Symbol	Description	Rating	Unit
Vdd	Supply Voltage	-0.5 ~ +3.6	V
Vin	Input Voltage	-0.5 ~ VDD +0.5	V
Vout	Output Voltage	-0.5 ~ VDD +0.5	V
Topr	Operation Temperature	-20~ 75	℃
Tstg	Storage Temperature	-40 ~ 125	℃
ESD	ESD Protection human mode	3	KV

9 Ordering Information

Part Number	Pin Count	Package
DM130256W	-	Wafer (Pb-Free)
DM130256	281	Dice (Pb-Free)

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Conditions beyond those listed for the absolute maximum may destroy or damage the products. In addition, conditions for sustained periods at near the limits of the operating ranges will stress and may temporarily (and permanently) affect and damage structure, performance and function.